

ADC performance in bench tests

BNL DUNE

David Adams

BNL

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Introduction

I have been looking at ADC test data taken at BNL

- I report here on data taken in January 2017
 - ADC samples are read out for input voltage steps with sawtooth envelope
 - 20M samples for each ADC channel
 - approximately 4k samples for each ADC bin
- Data is from P1 chips
 - 35-ton used an earlier version
 - Expect this chip will be used for protoDUNE
- Data taken under different conditions
 - Warm (room temp) and cold (LN2)
 - Different sampling rates (1 and 2 MHz)
 - I show results for 2 MHz cold
 - All data taken with external clock

Data taking

Data taken by the following team

- Hucheng Chen, Shanshan Gao, Jack Fried, Feng Liu (BNL)
- Damian Goeldi (Univ. of Bern)

Thanks to them to making this data available to me

Data format

- ADC samples
- Input voltage ramp from -200 to 1800 mV in 10 s

Data taken for 25 ADC chips

- 16 channels each
 - I.e. a total of 400 ADC channels
 - And a total of 1.6M ADC bins (4096 bin/codes per channel)
- Chip placements:
 - Chip 0 is bare
 - Chips 2 and 4 are in board
 - Remainder are in a socket

Response

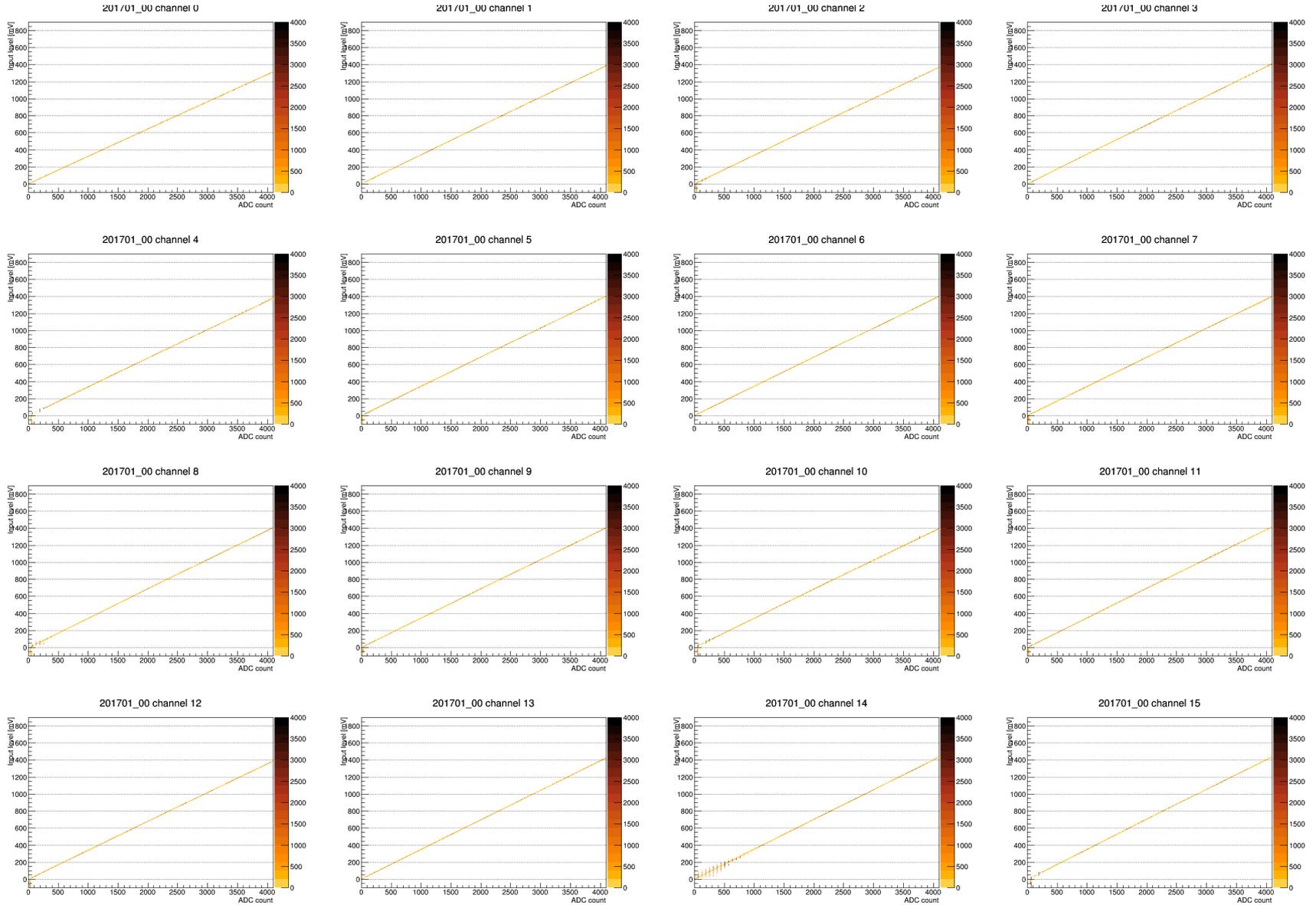
Following slides have response plots

- Input signal vs. ADC signal
- For chips 0 and 6
- Note the second has a voltage offset for some of the channels

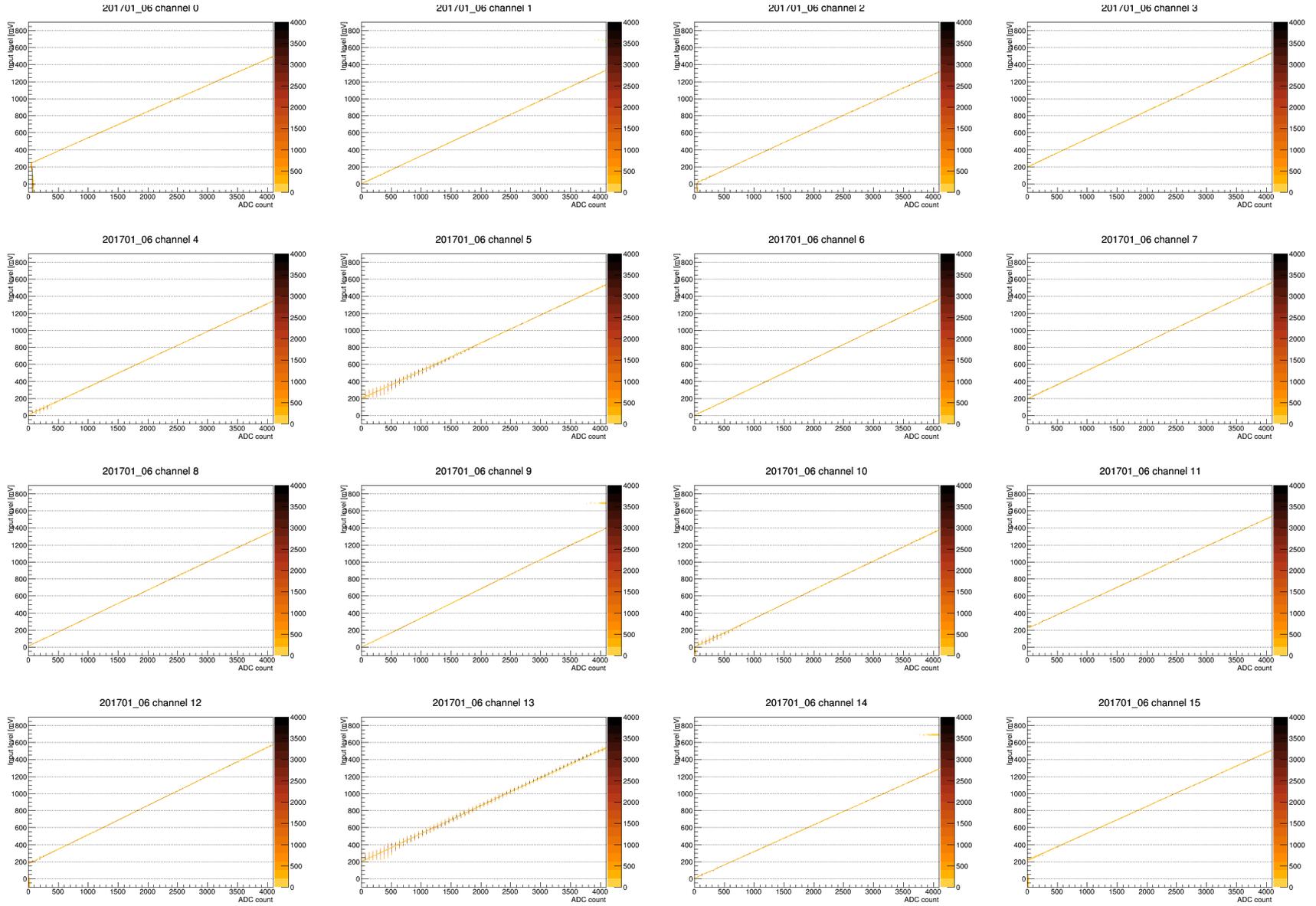
Comments

- Plots look linear by eye (linear fit residuals in appendix)
- Often problems in lower ADC codes
 - Below 64 or 200 or 500+

ADC 0



ADC 6



Fits and residuals

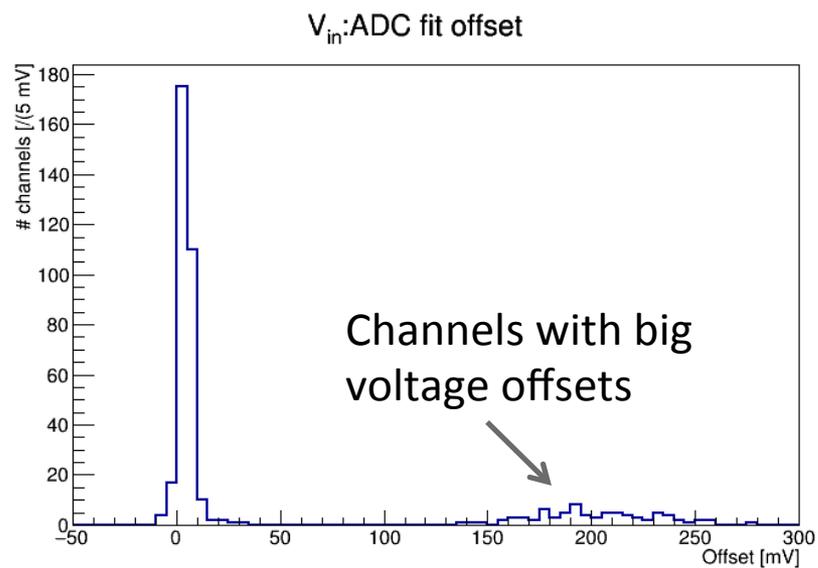
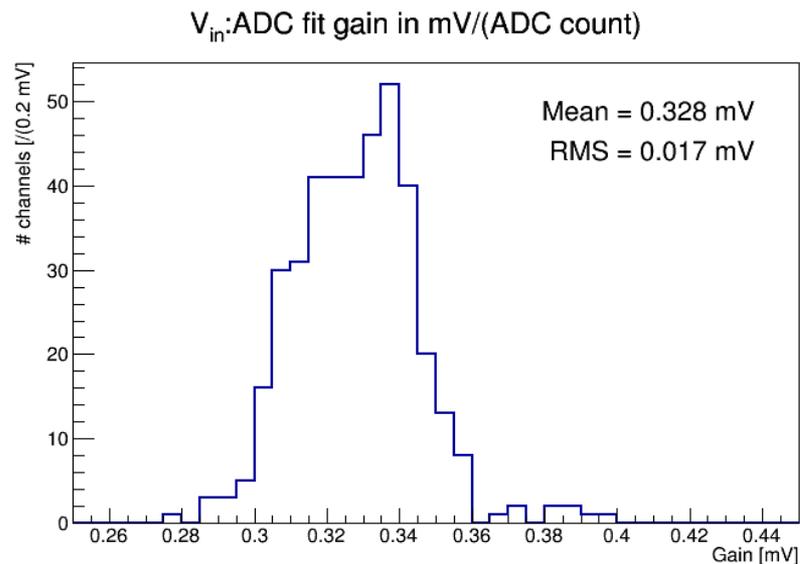
Linear fits

- I make a linear fit of the inverse response for each channel
 - $V_{in} = \text{gain} \times (\text{ADC code}) + \text{offset}$
- Gain varies by $\pm 5\%$ (RMS)
 - So we need a separate calibration for each channel
- Response show significant non-linearities
 - Evident in residual plots in appendix
 - Residual = difference between true and fitted V_{in}
 - Plots show this residual for each ADC bin
- In addition, there are sticky bins
 - I.e. ADC codes for which a wide range of input voltages contribute
 - Vertical lines in the response and residual plots

Fitted parameters

Results of fits at right

- Top is distribution of fitted gains
- Bottom is offsets



Resolutions

We extract stats from the residual plots

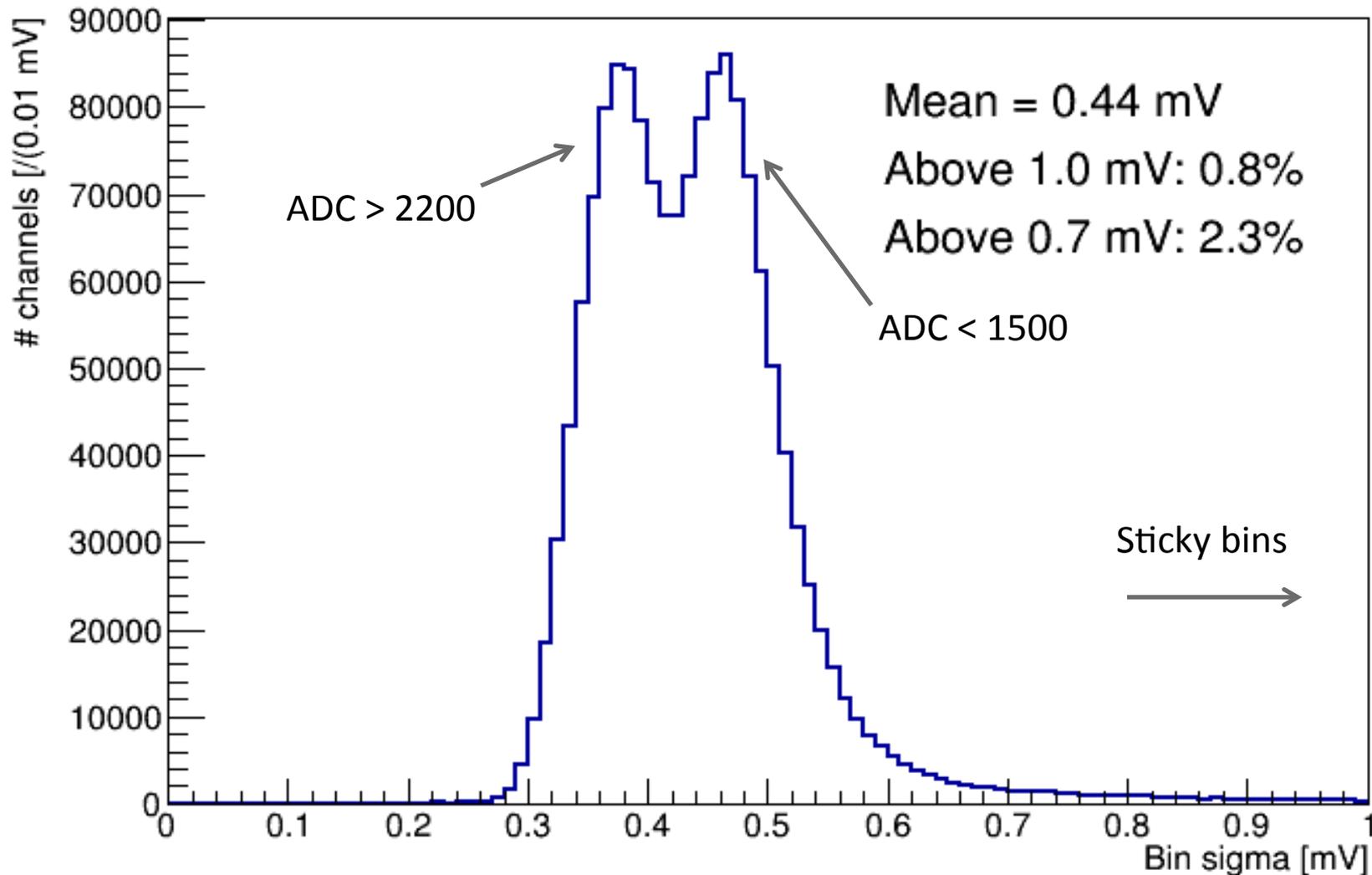
- Mean for each ADC bin
 - This is the “ultimate” calibration
- RMS of the deviation from zero
 - This is the resolution we get with the linear calibration
 - Not presented here—see earlier talks
- Standard deviation (σ) is the RMS of deviation from its mean
 - This is the resolution we get with ultimate calibration

Ultimate resolution

- I.e. that obtained with the ultimate calibration
- Varies from bin to bin
- Large for sticky bins
- Distribution for all bins on following slide

Ultimate resolution

ADC bin resolution distribution ($64 < \text{ADC} < 4095$)



Metrics

Want to develop metrics to characterize ADC quality

- So we can decide which chips to use in protoDUNE
- Plan to produce 3000 chips and select 1000 for the detector

Voltage range covered by the chip

- May be different for each channel on a chip
 - Some have 200 mV offset and some don't
- I use the the endpoints of linear calibration to evaluate this range
- ADC bin 65 for the low end because lower bins are often bad
- ADC bin 4094 for the high end (4095 is overflow)
- See plot on following page

Fraction of bins with bad resolution (i.e. that are sticky)

- Define bad with a cut on the (ultimate) resolution
- Note that 1 mV corresponds to
 - $(6240 \text{ e/fC}) / (14 \text{ mV/fC}) = 450 \text{ e}$

Metrics (2)

Following slide shows these two metrics

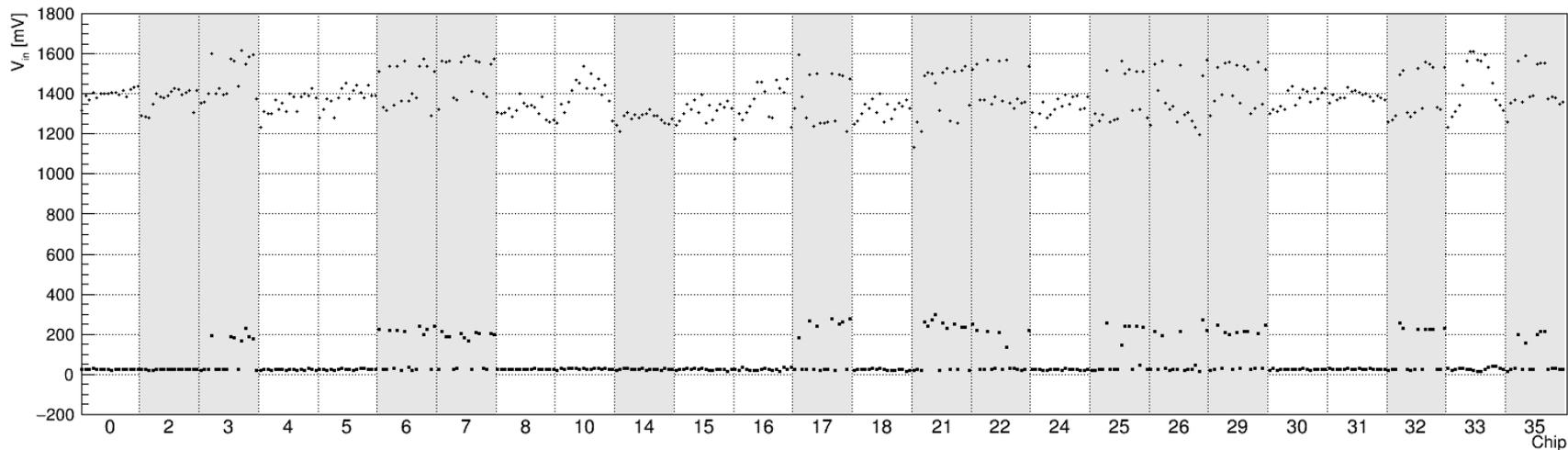
- For each channel
 - Chip number is on the x-axis
- Lower and upper voltage limits
- Fraction of bad channel for two thresholds
 - 0.8 mV (360 e)
 - 1.2 mV (530 e)

Better channels are shown with white BG

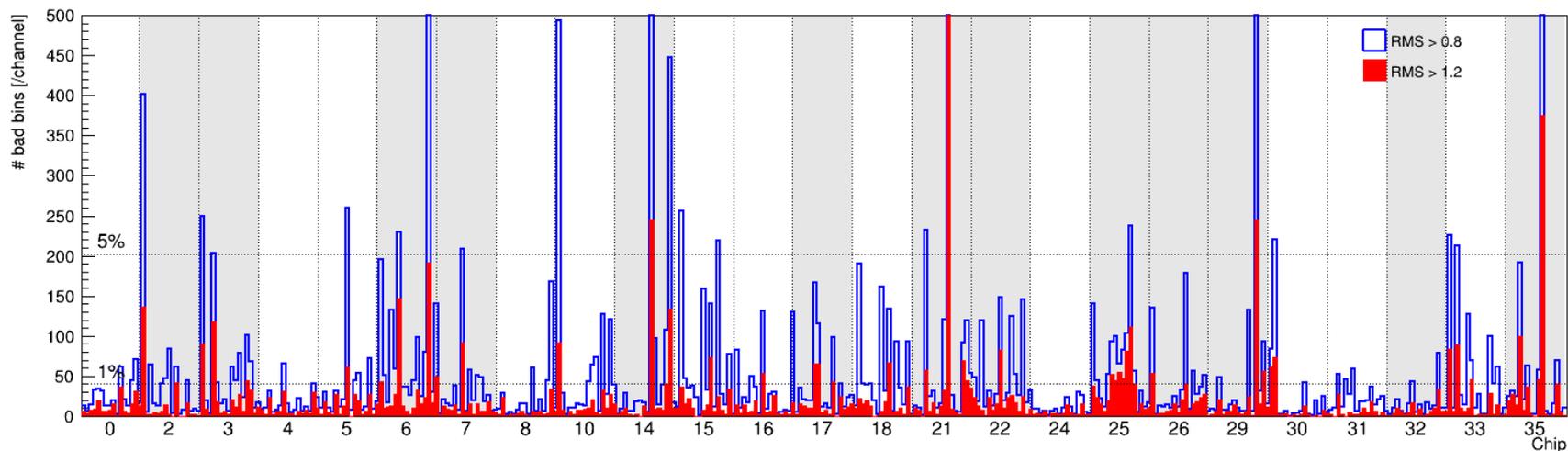
- Range close to (0, 1200) mV for all channels
- I selected 12 chips (to get the desired yield)
 - Require all channels for each to be “good”
 - About 1/2 of the studied sample (25 chips)
 - About 1/3 of the 35 fabricated
 - Remaining 10 could not be used
 - Possible to recover these with extra effort?

Metrics (3)

Input voltage limits for $64 < \text{ADC} < 4095$



ADC bad bin distribution ($64 < \text{ADC} < 4095$)

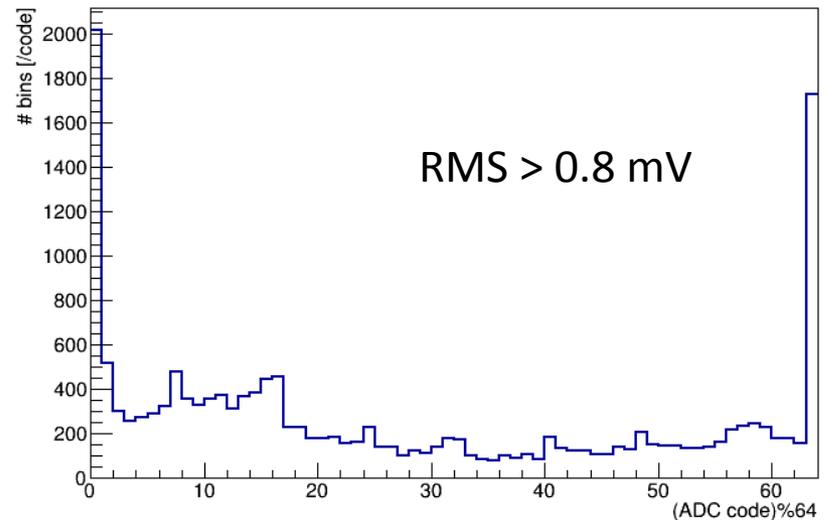


Sticky codes

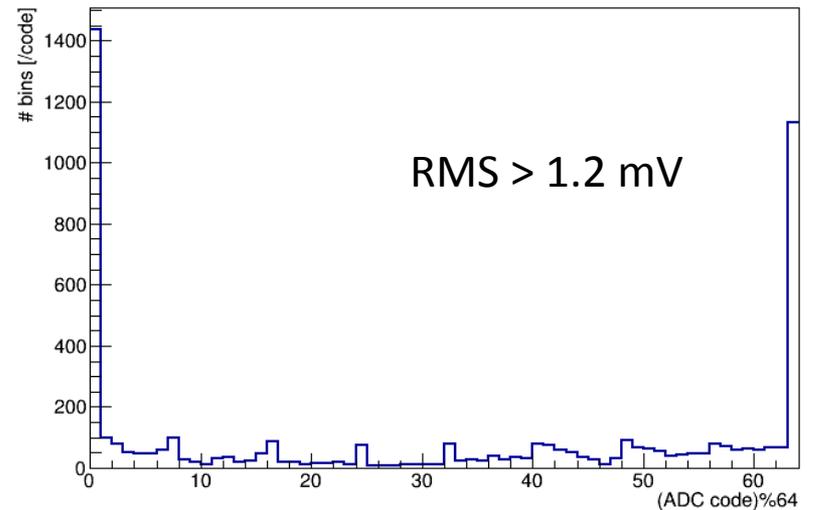
Which codes are sticky?

- Plots at right show the the 6 LSB (least significant bits) for the bad bins
 - For each of the two thresholds
- Often but not always the classic values of 0 and 63

ADC bad code distribution (512 < ADC < 4095, RMS > 0.8 mV)



ADC bad code distribution (512 < ADC < 4095, RMS > 1.2 mV)



More metrics

Like to go beyond the metrics presented here

- What is the likelihood that a give input voltage will give a useful ADC measurement?
 - May be quite different from the fraction of good bins
 - May show that the useful voltage range is smaller (or larger) than that shown here
- I plan to evaluate this with the existing data
 - Stay tuned...

Comments and conclusions

ADC response

- ADCs show non-negligible nonlinearities
 - We will want many-parameter calibration for each channel
 - 4000 parameters (one/bin) for ultimate calibration
- In addition there are bins that cannot be used
 - Populated by a wide range of input voltages (sticky)
 - Identified by poor “ultimate” resolution
- Resolution is typically 0.5 mV (230 e) with a few % of bins much higher
 - Not so easy to find chips where all 16 channels are like this

Metrics

- Presented a couple metrics today (both for each channel)
 - Voltage range from linear fit
 - Fraction of bad channels (identified with threshold on ultimate resolution)
- Plan to look at efficiency vs. input voltage
- Use these metrics to identify the better chips

Future studies

- Correlations in time (tick-to-tick)
- Change in response and bad channels with time (week, month, ...)

Appendix

Effective # bits

Voltage response for some example bins

- Mostly sticky

Residual plots for all chips follow

Effective number of bits

Sometimes useful to characterize ADC with effective # bits, N_e :

$$\sigma_V = \sigma_0 2^{(12-N_e)}$$

where σ_V is the measured resolution (on the input voltage)

and σ_0 is the ideal resolution:

$$\sigma_0 = g/\text{sqrt}(12) = (0.328 \text{ mV})/\text{sqrt}(12) = 0.095 \text{ mV}$$

using the average gain for the ADCs analyzed here.

The effective # bits is then

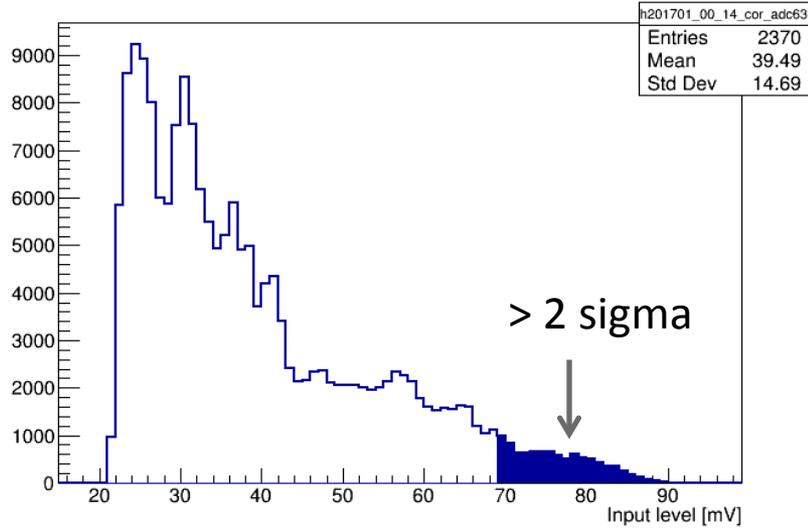
$$N_e = 12 - \log(\sigma_V/\sigma_0)/\log(2)$$

Table shows effective # bits

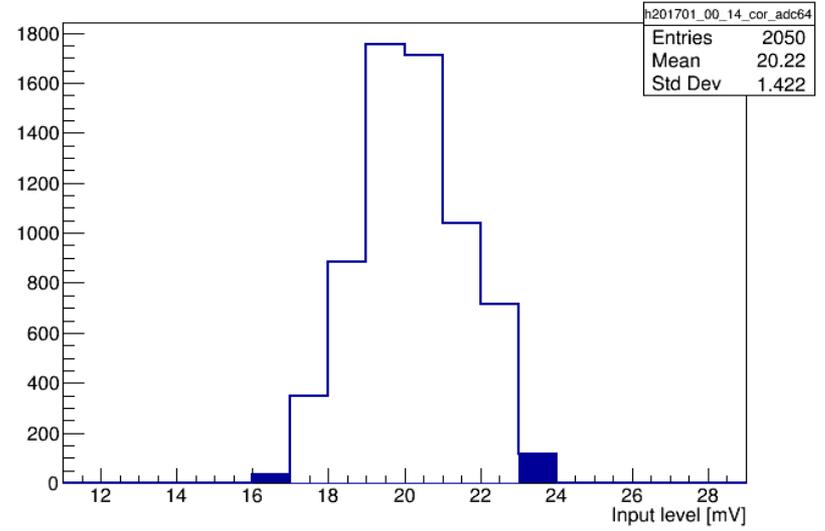
- For various resolutions
- The effective # bits for the good bins here are 9-10

N	σ_V (mV)
12	0.095
11	0.19
10	0.38
9	0.76
8	1.5
7	3.0
6	6.1

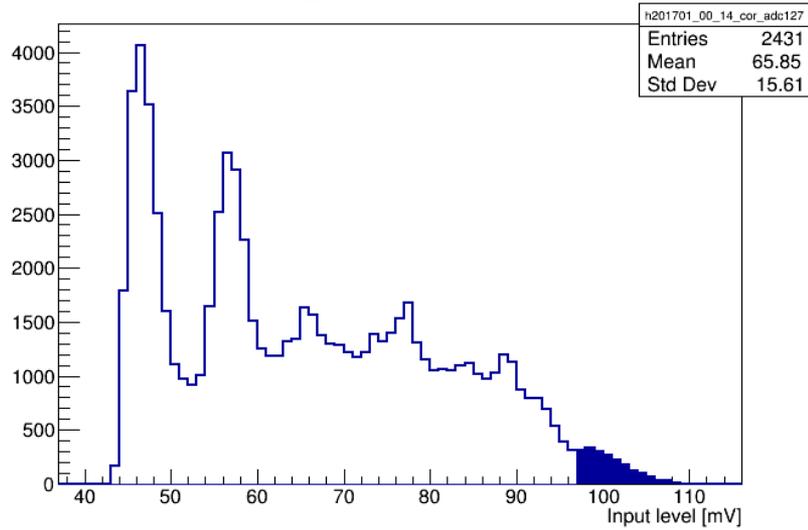
201701_00 channel 14 bin 63



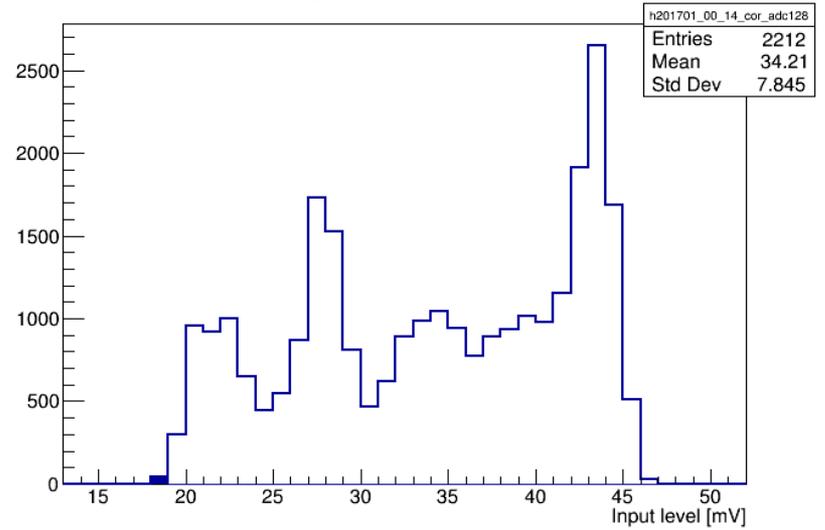
201701_00 channel 14 bin 64



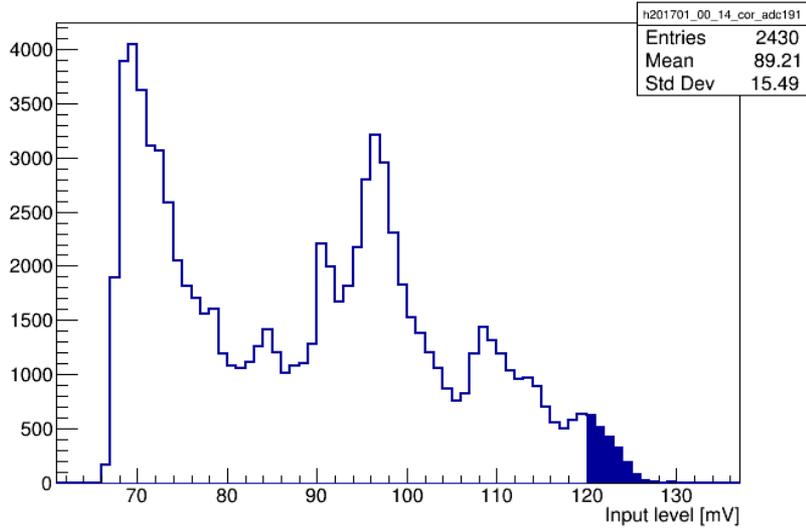
201701_00 channel 14 bin 127



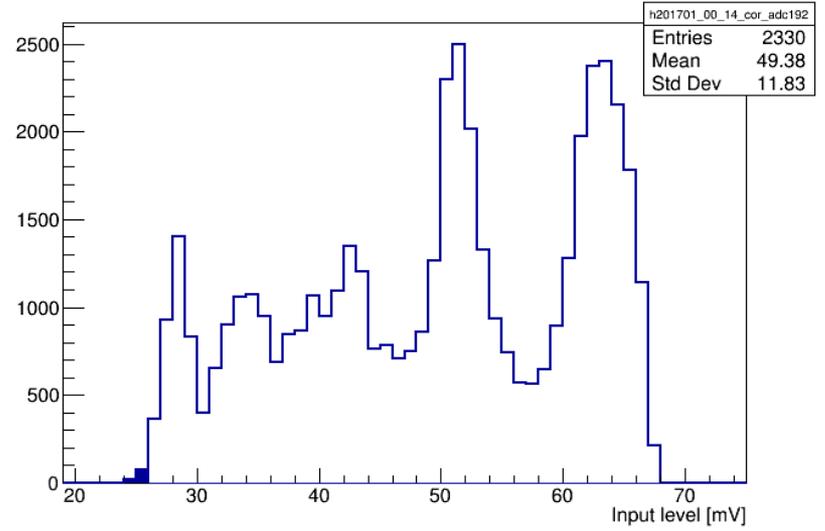
201701_00 channel 14 bin 128



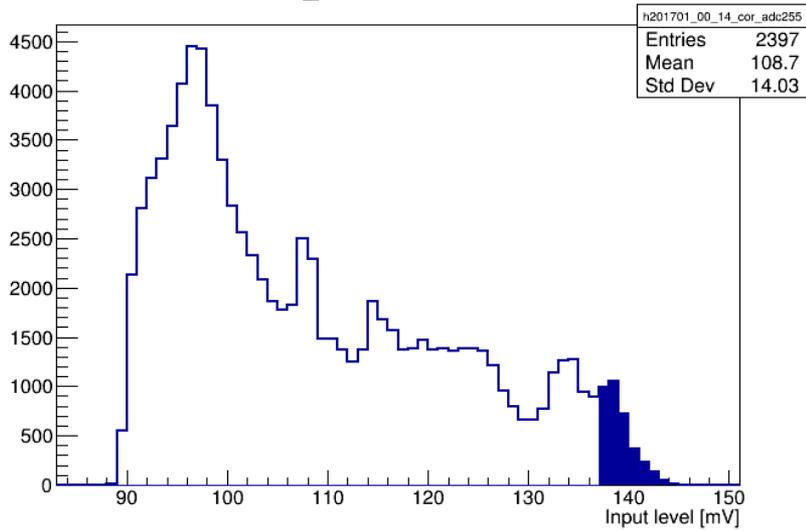
201701_00 channel 14 bin 191



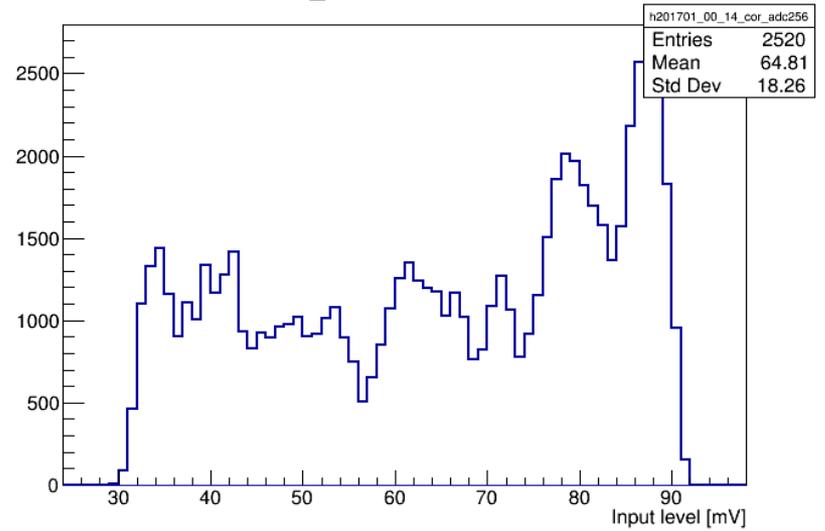
201701_00 channel 14 bin 192



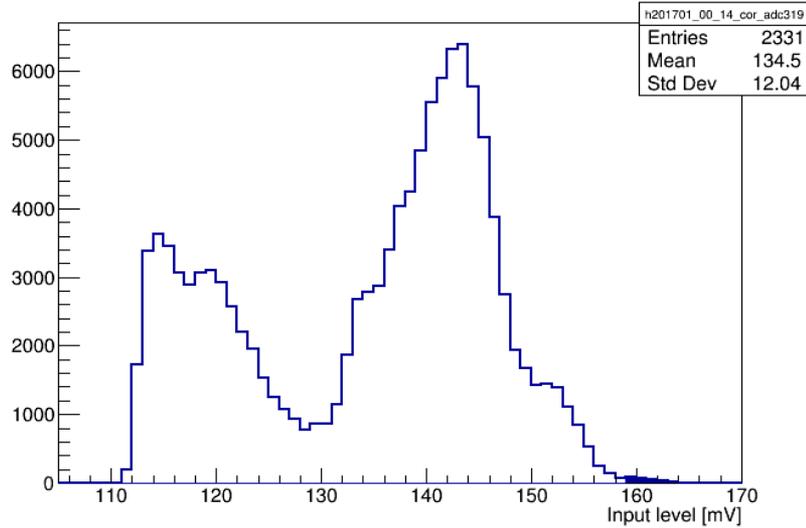
201701_00 channel 14 bin 255



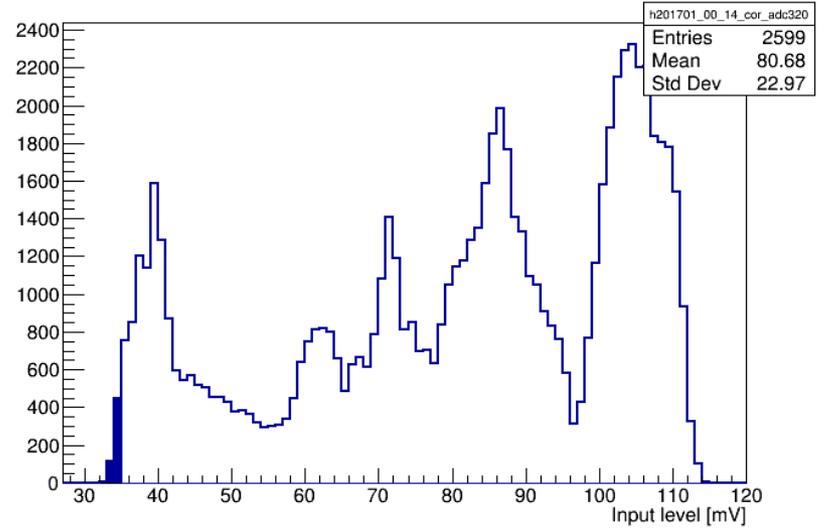
201701_00 channel 14 bin 256



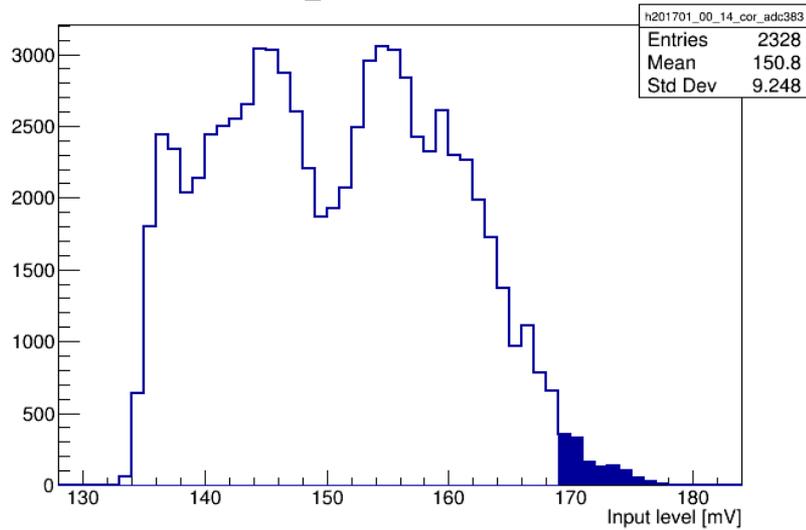
201701_00 channel 14 bin 319



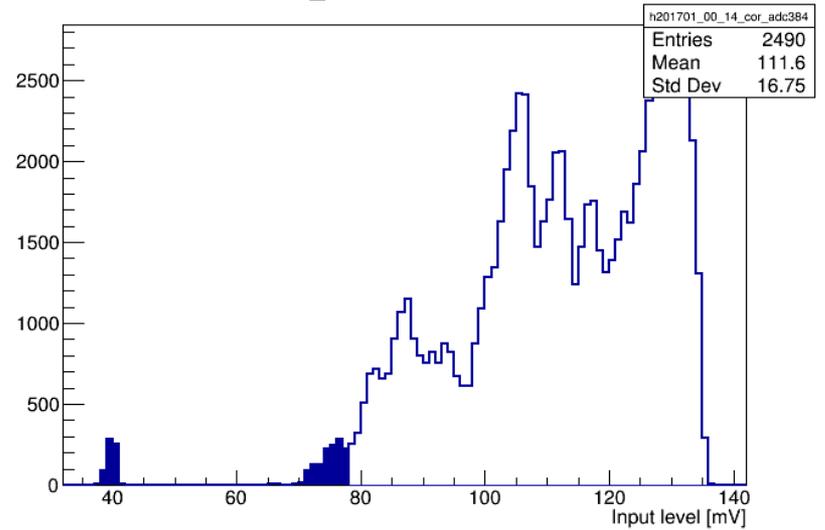
201701_00 channel 14 bin 320



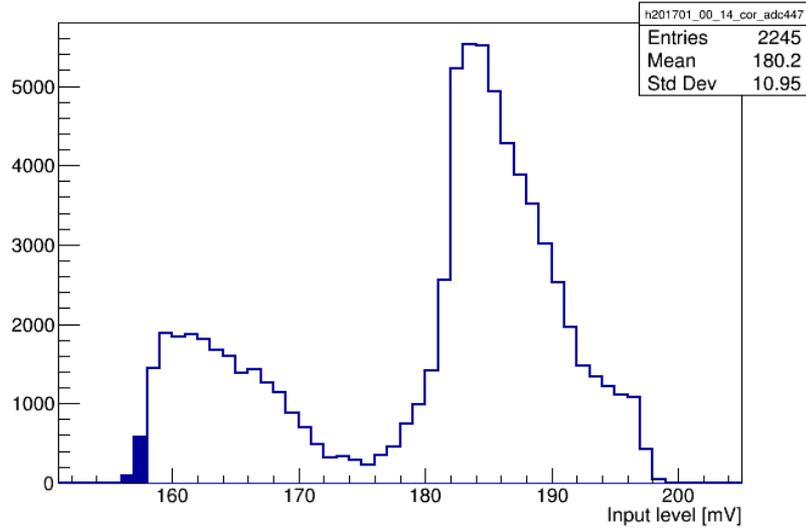
201701_00 channel 14 bin 383



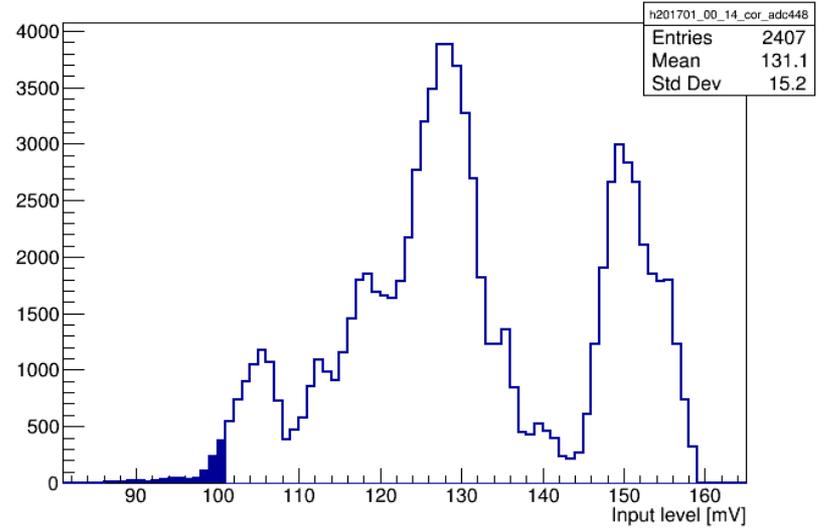
201701_00 channel 14 bin 384



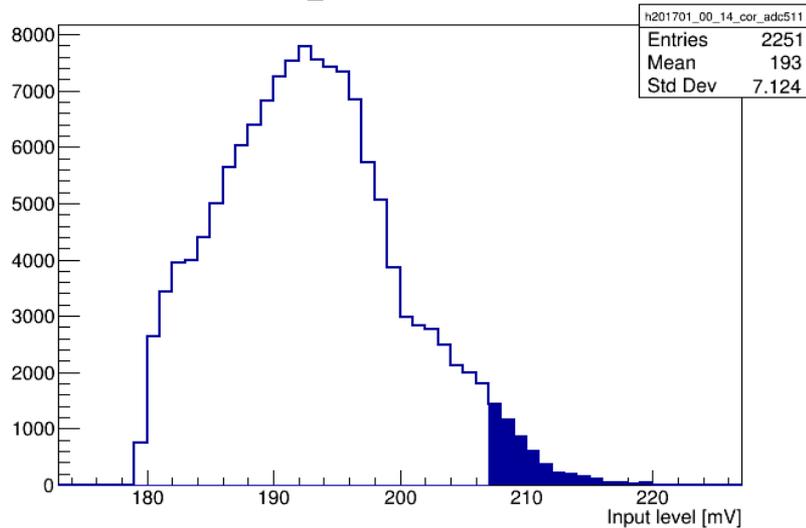
201701_00 channel 14 bin 447



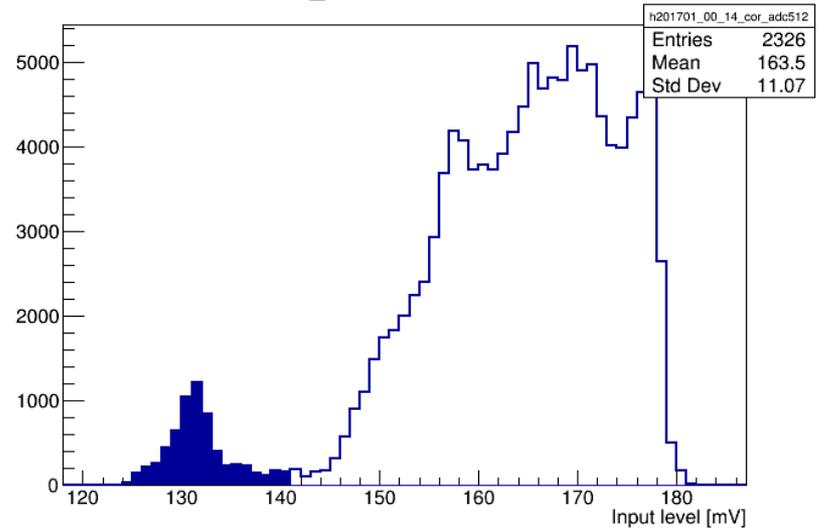
201701_00 channel 14 bin 448



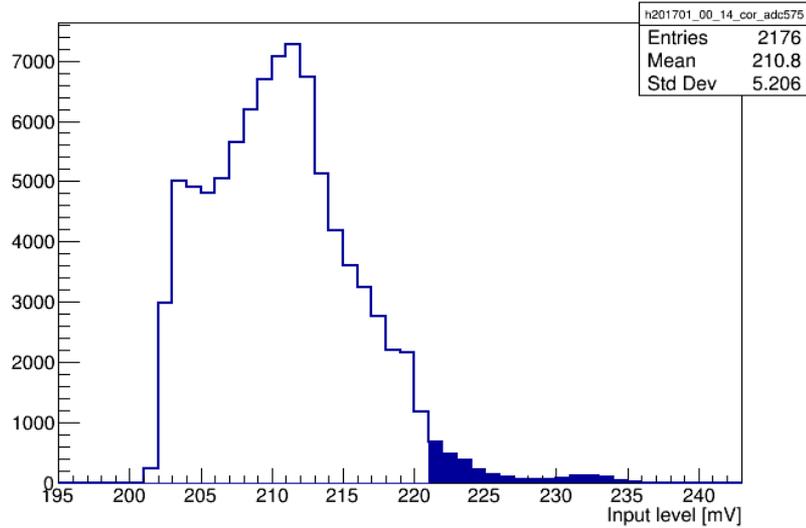
201701_00 channel 14 bin 511



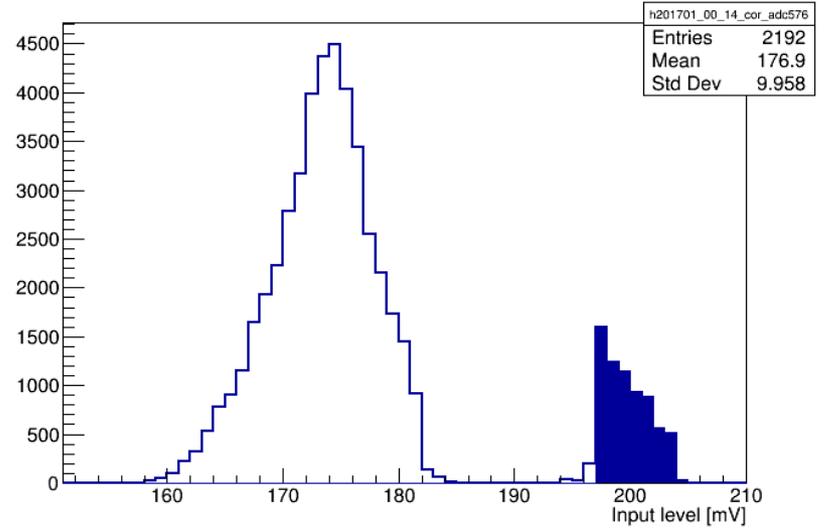
201701_00 channel 14 bin 512



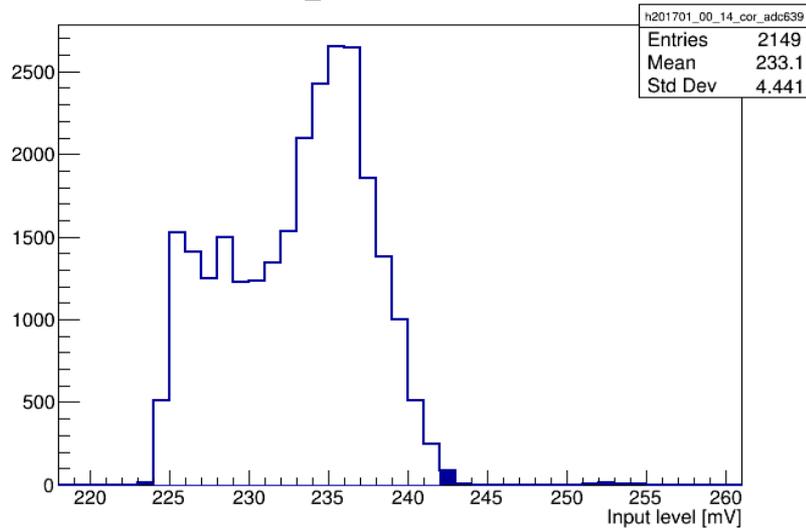
201701_00 channel 14 bin 575



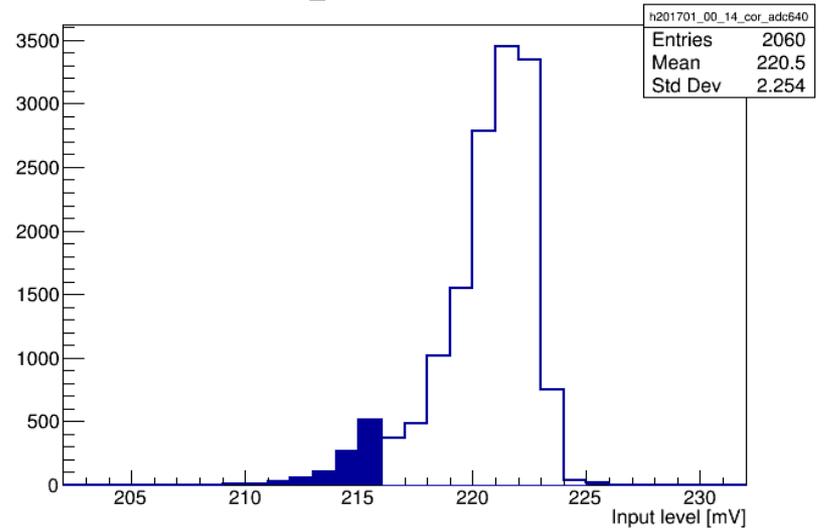
201701_00 channel 14 bin 576



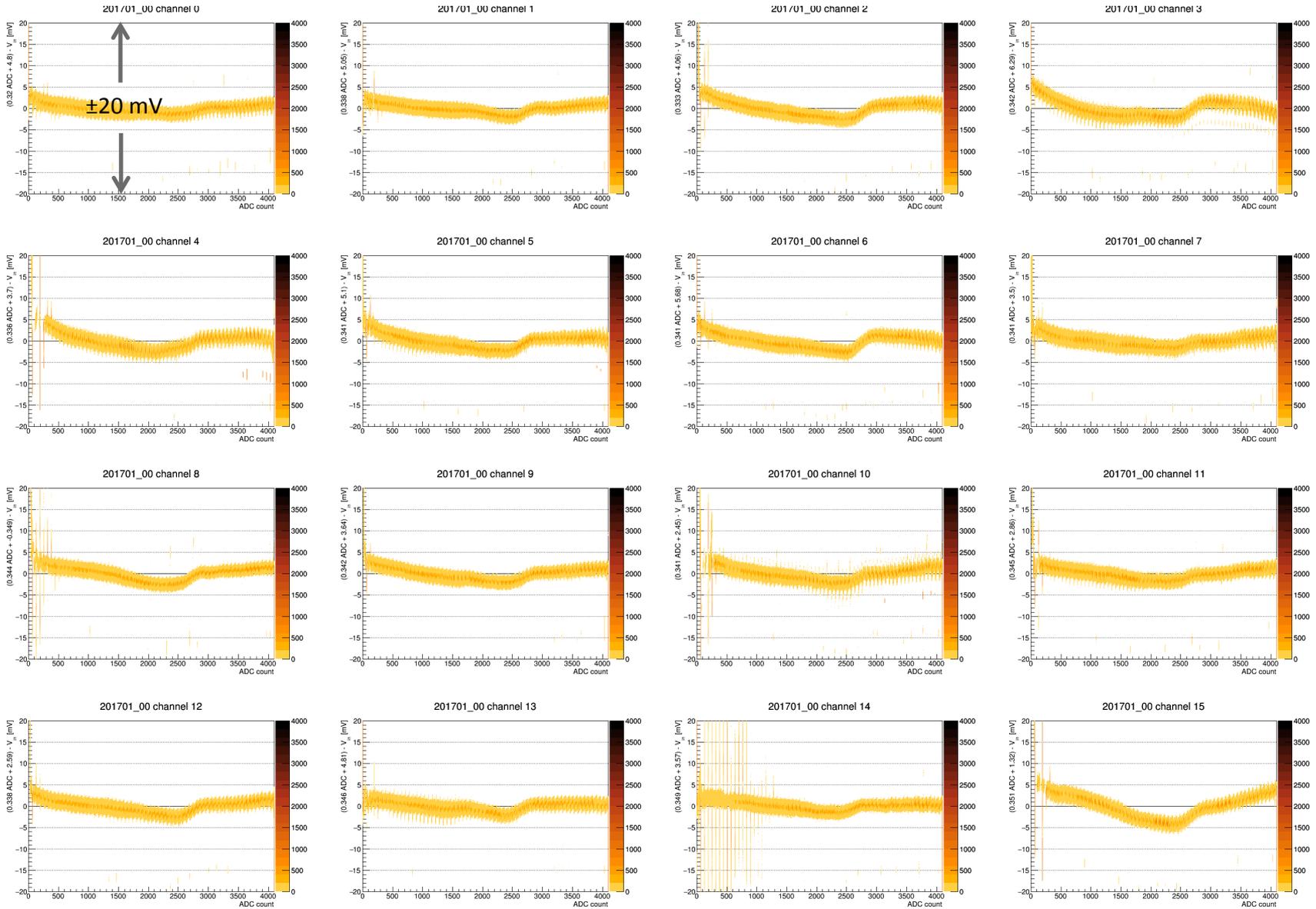
201701_00 channel 14 bin 639



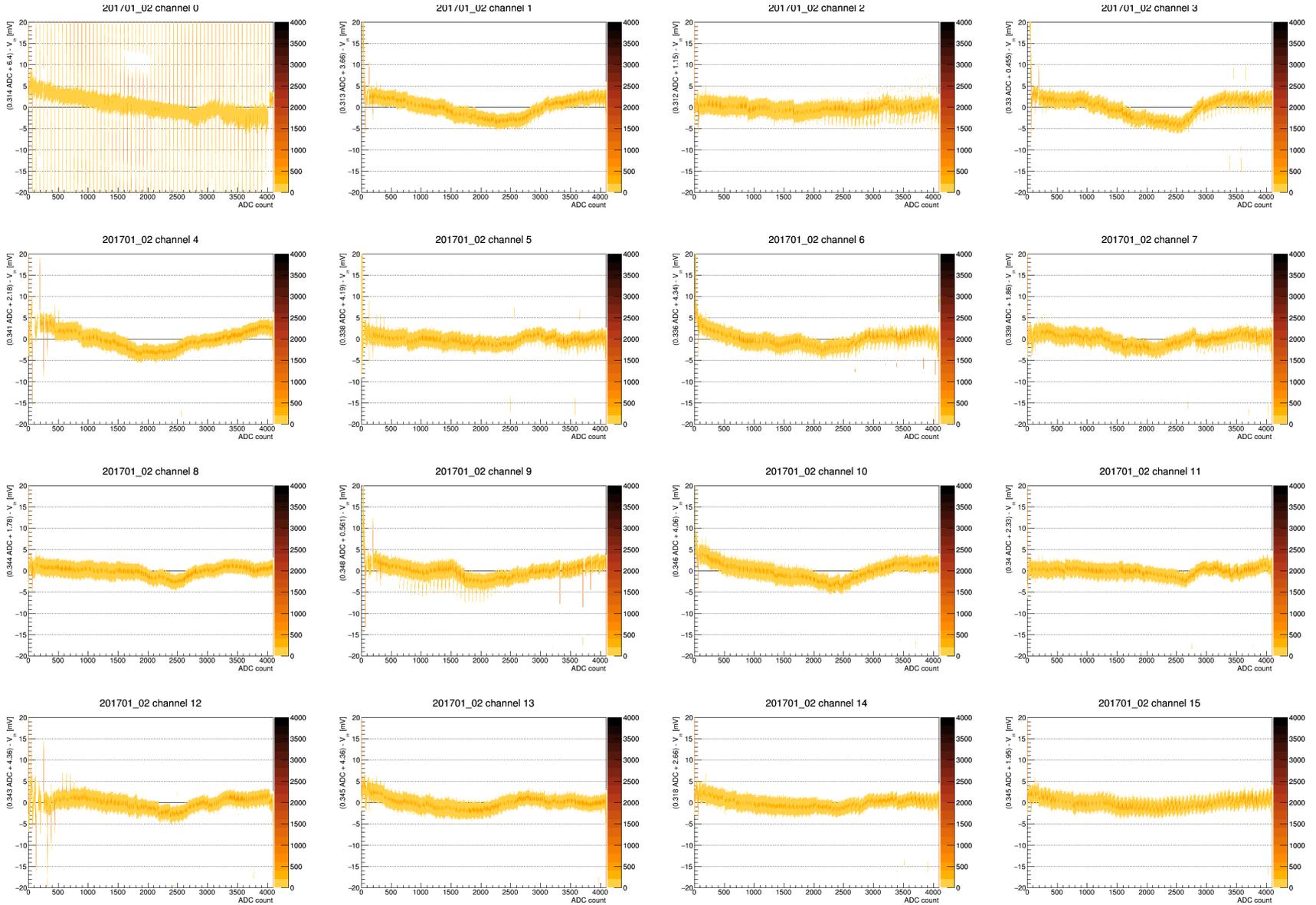
201701_00 channel 14 bin 640



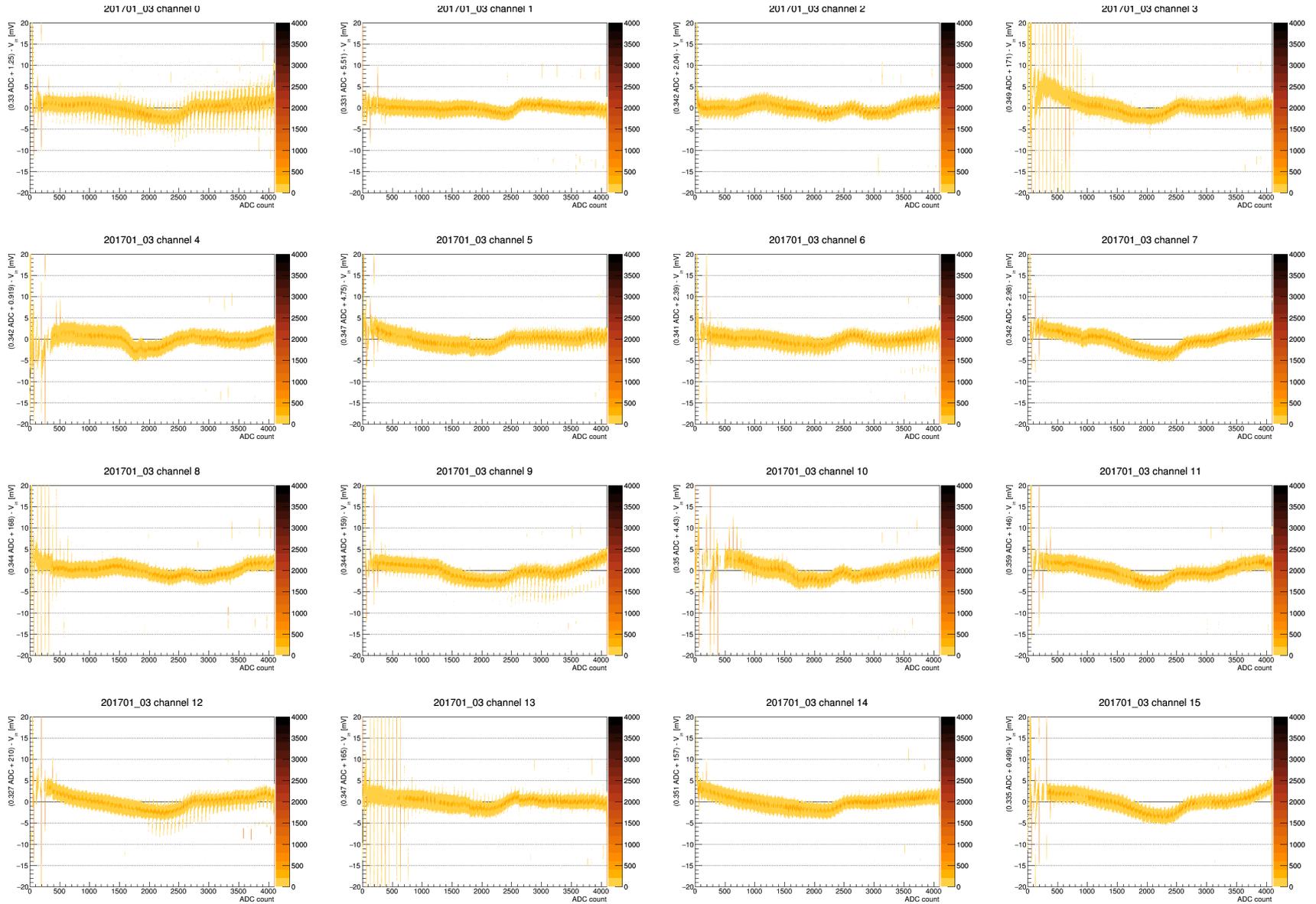
ADC 0 (bare)



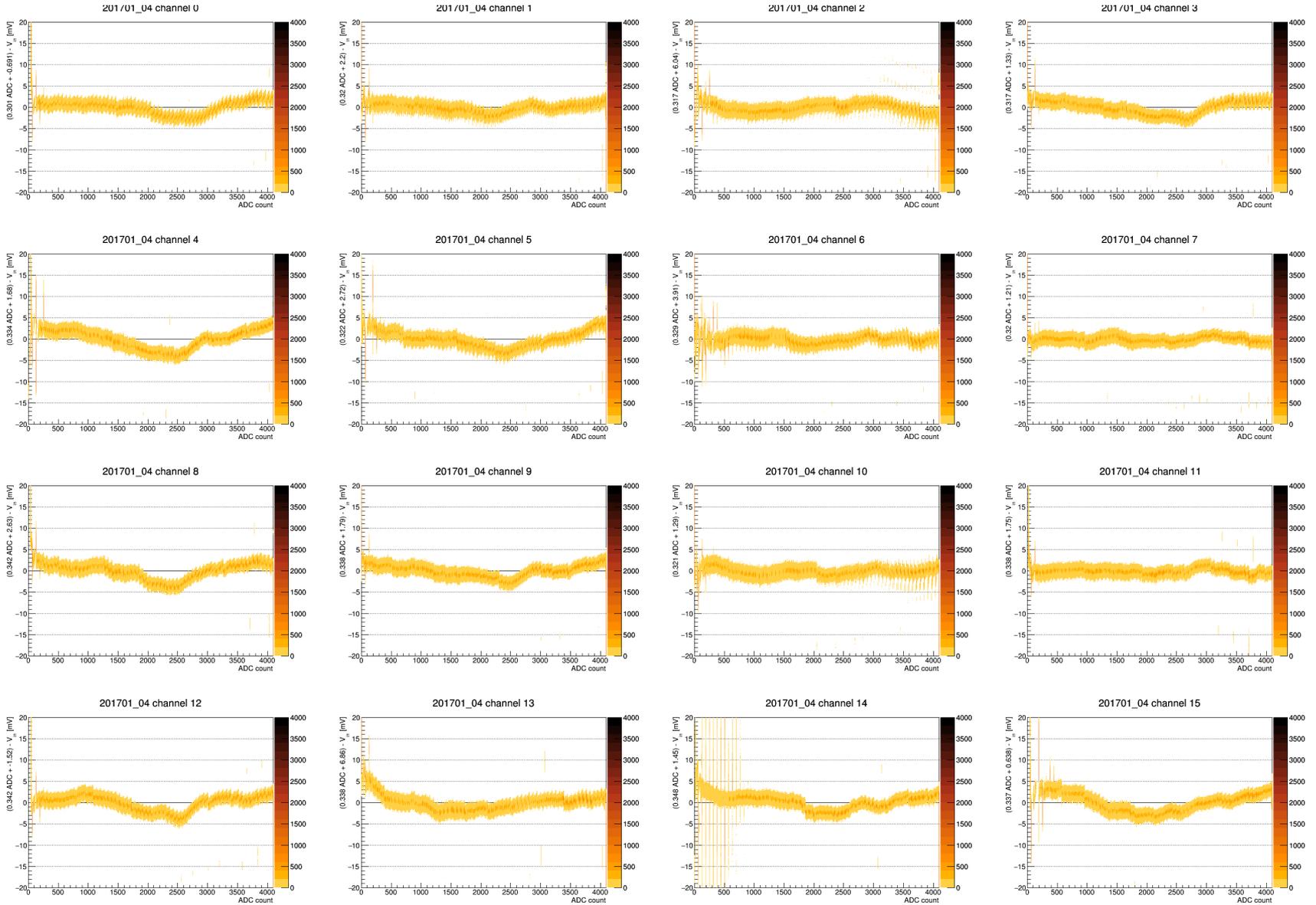
ADC 2 (board)



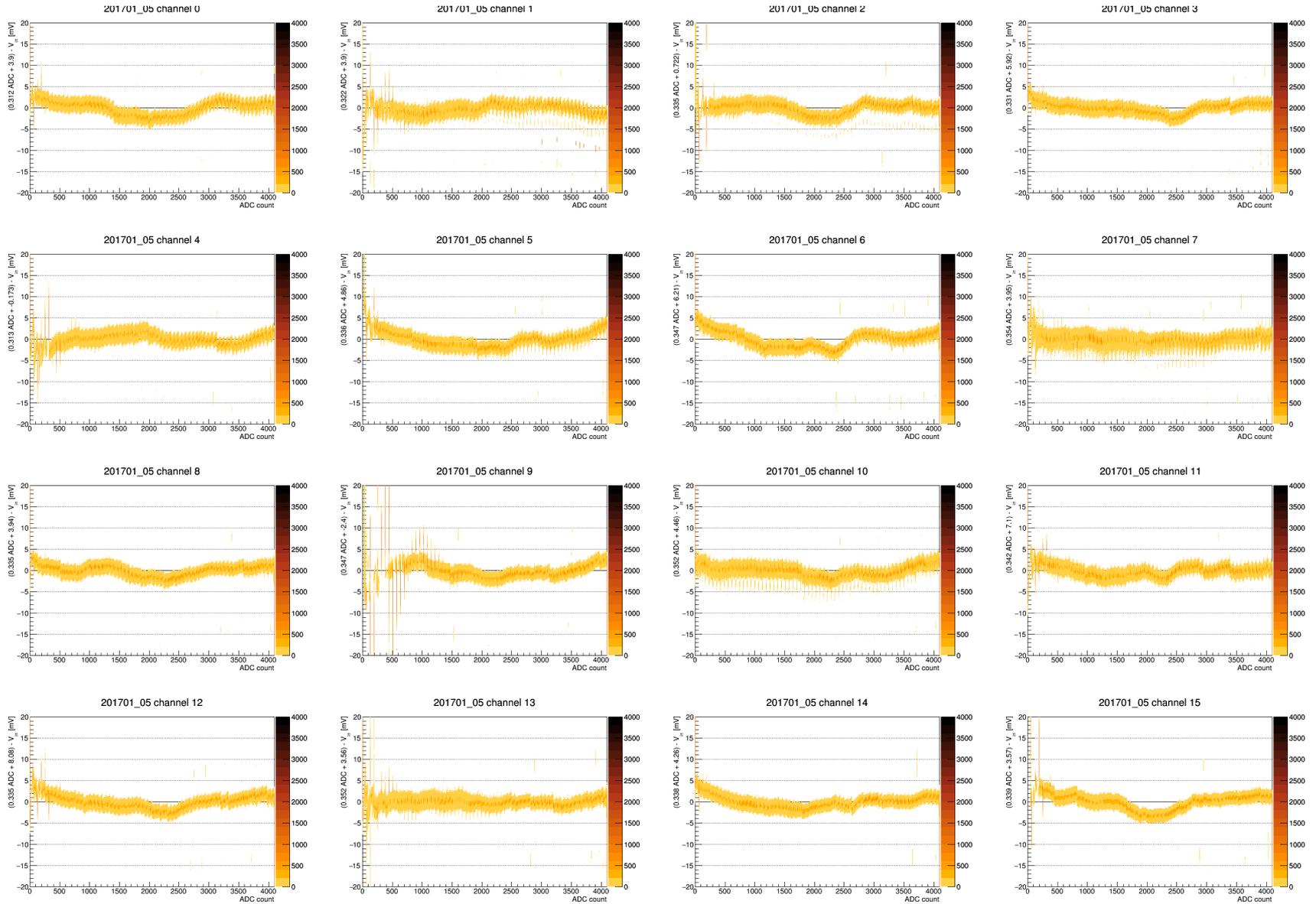
ADC 3



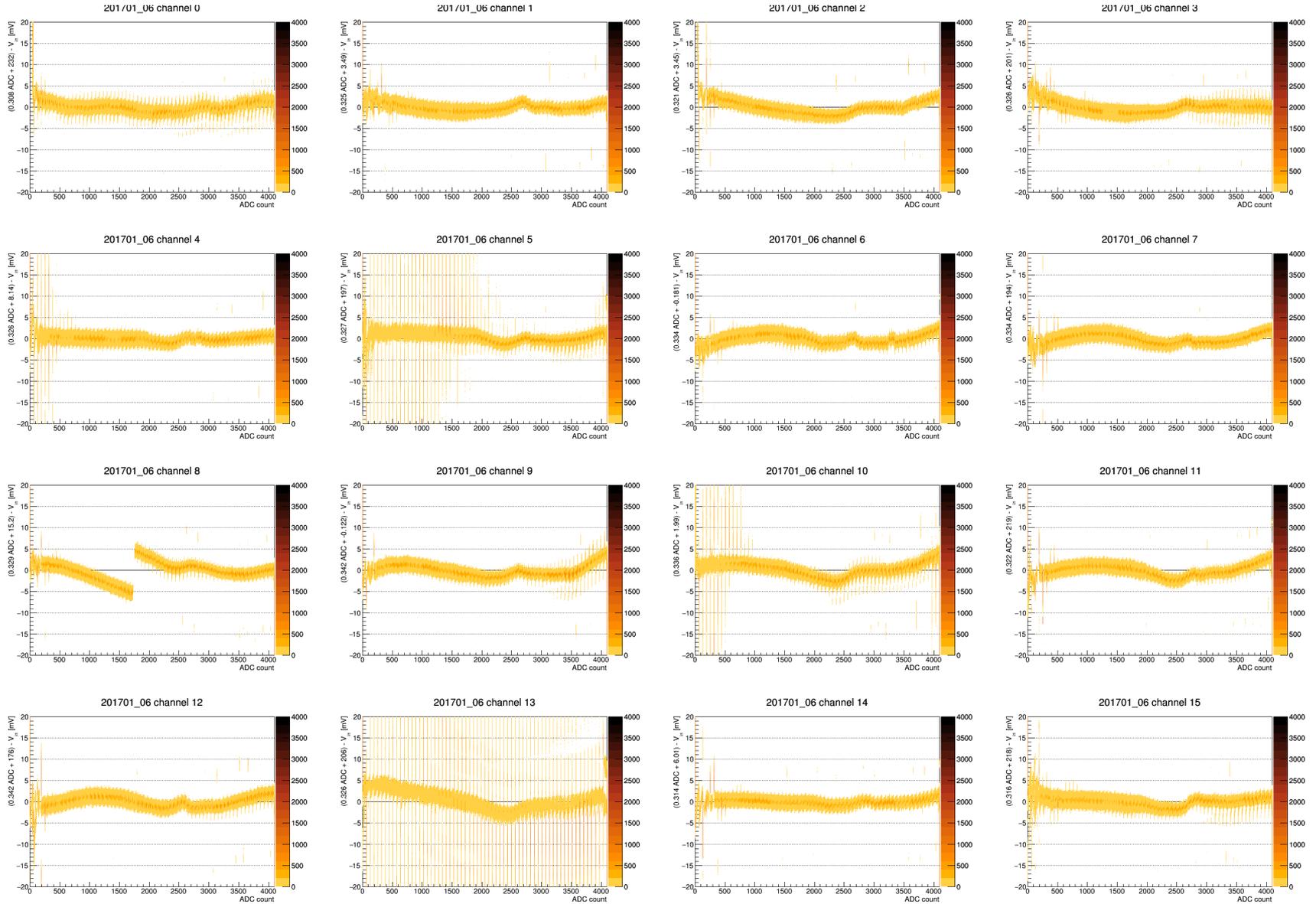
ADC 4 (board)



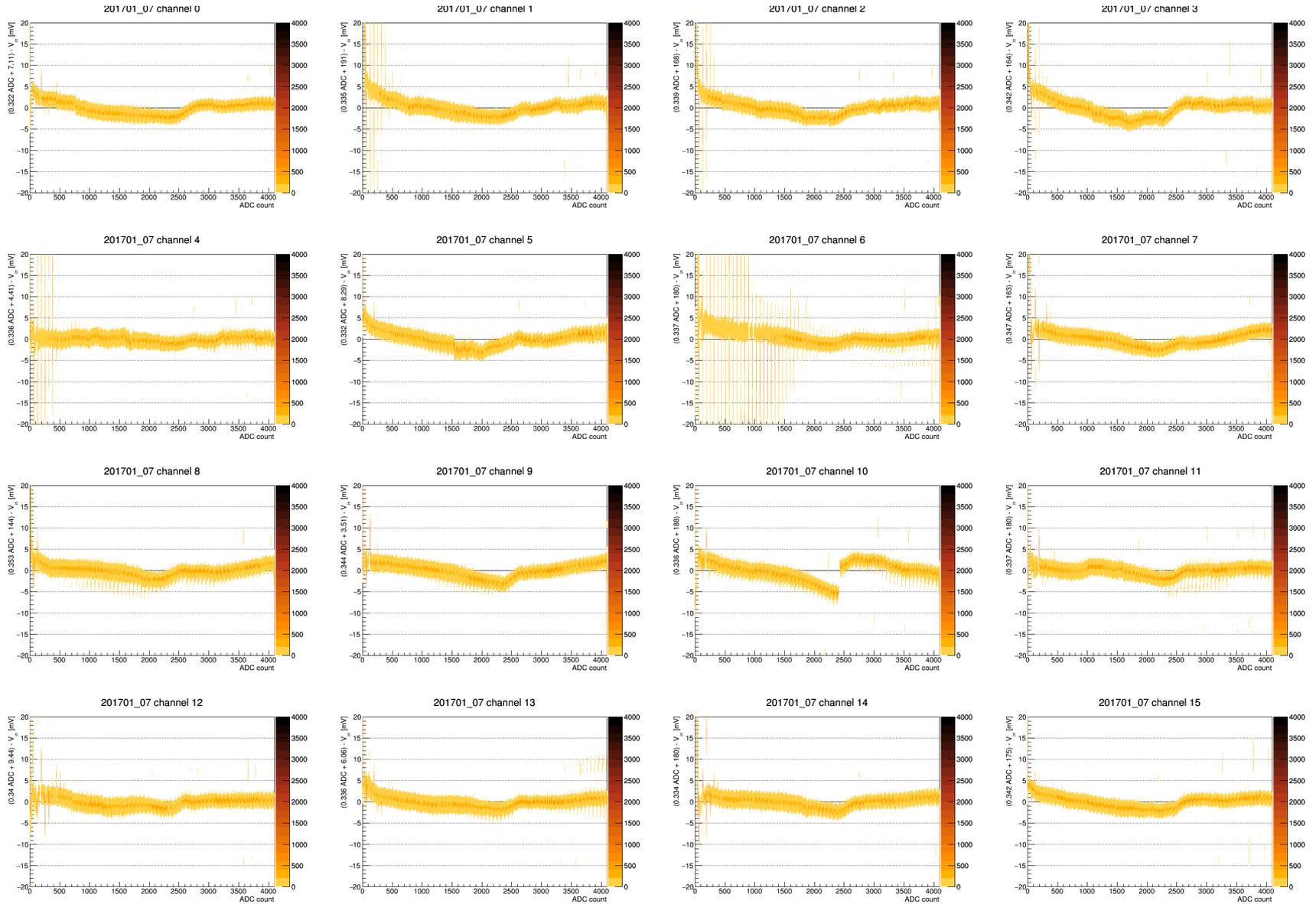
ADC 5



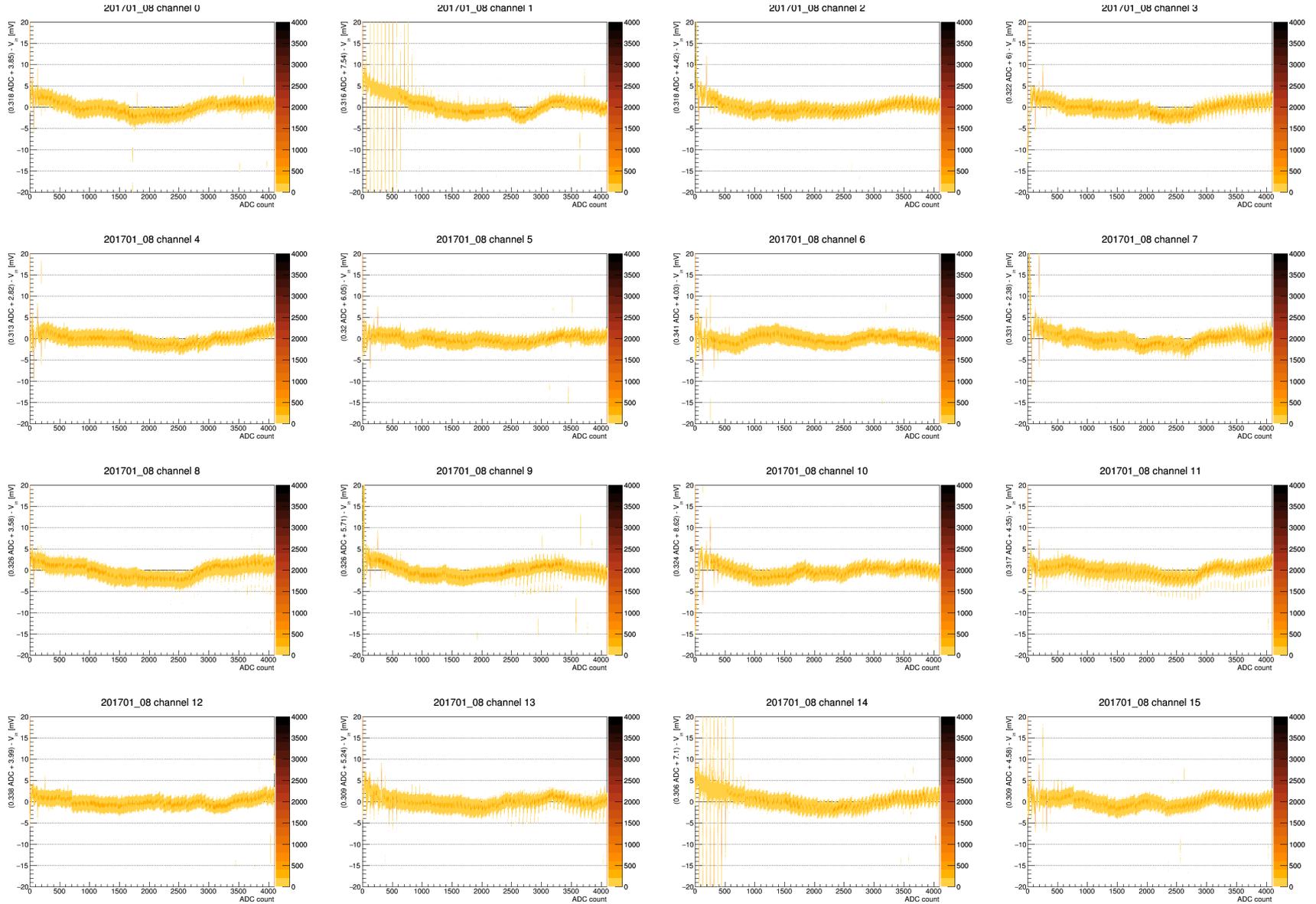
ADC 6



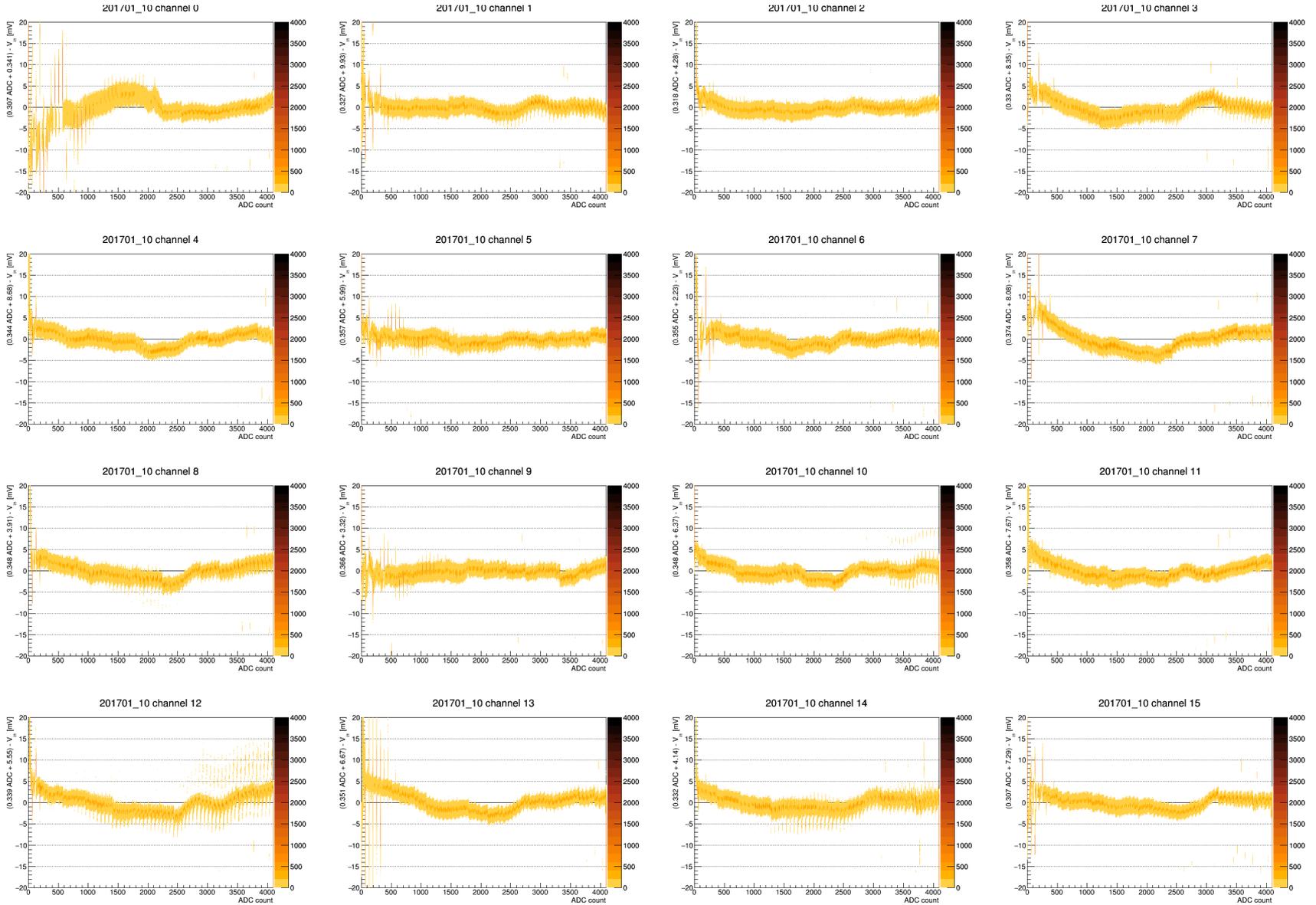
ADC 7



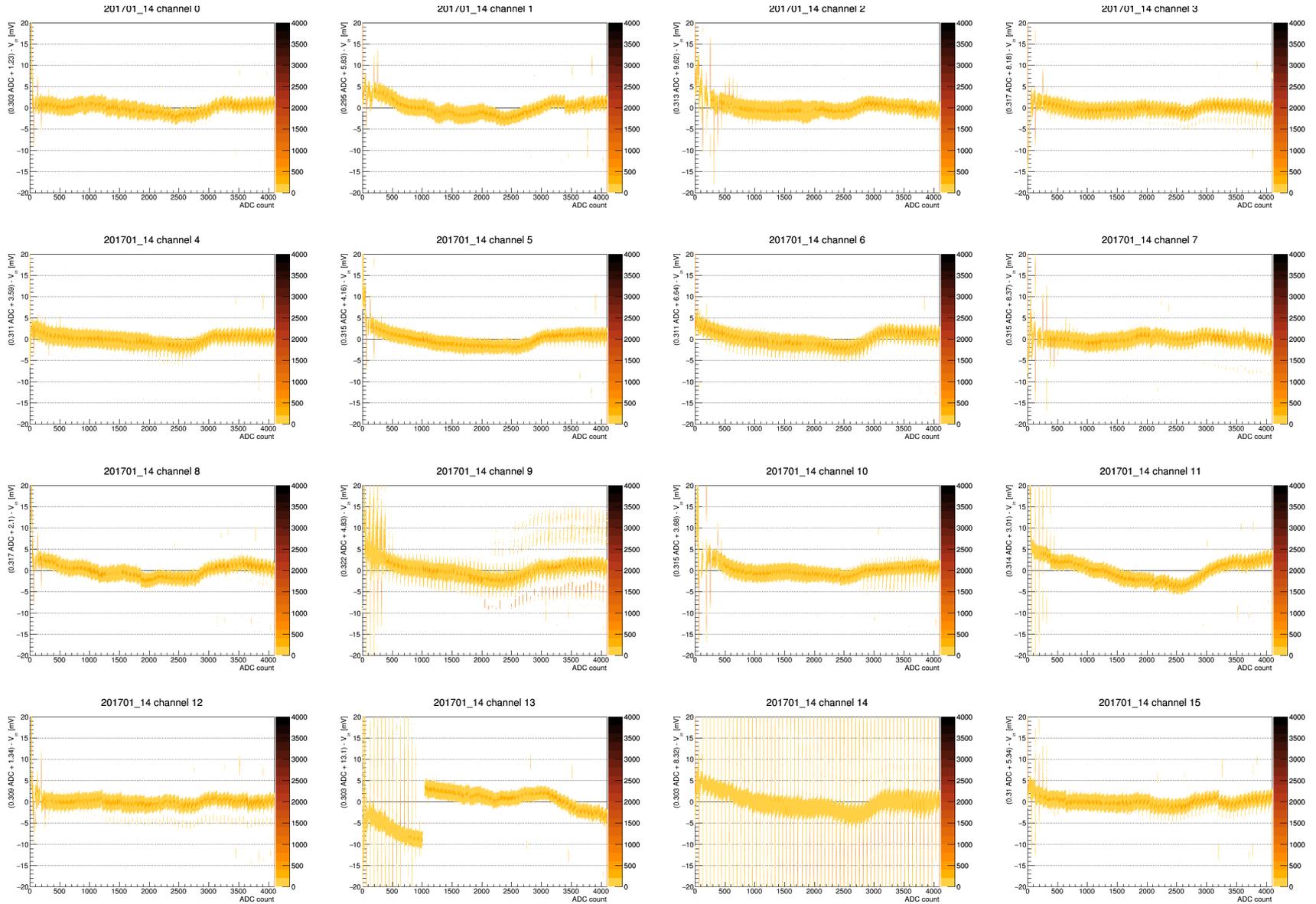
ADC 8



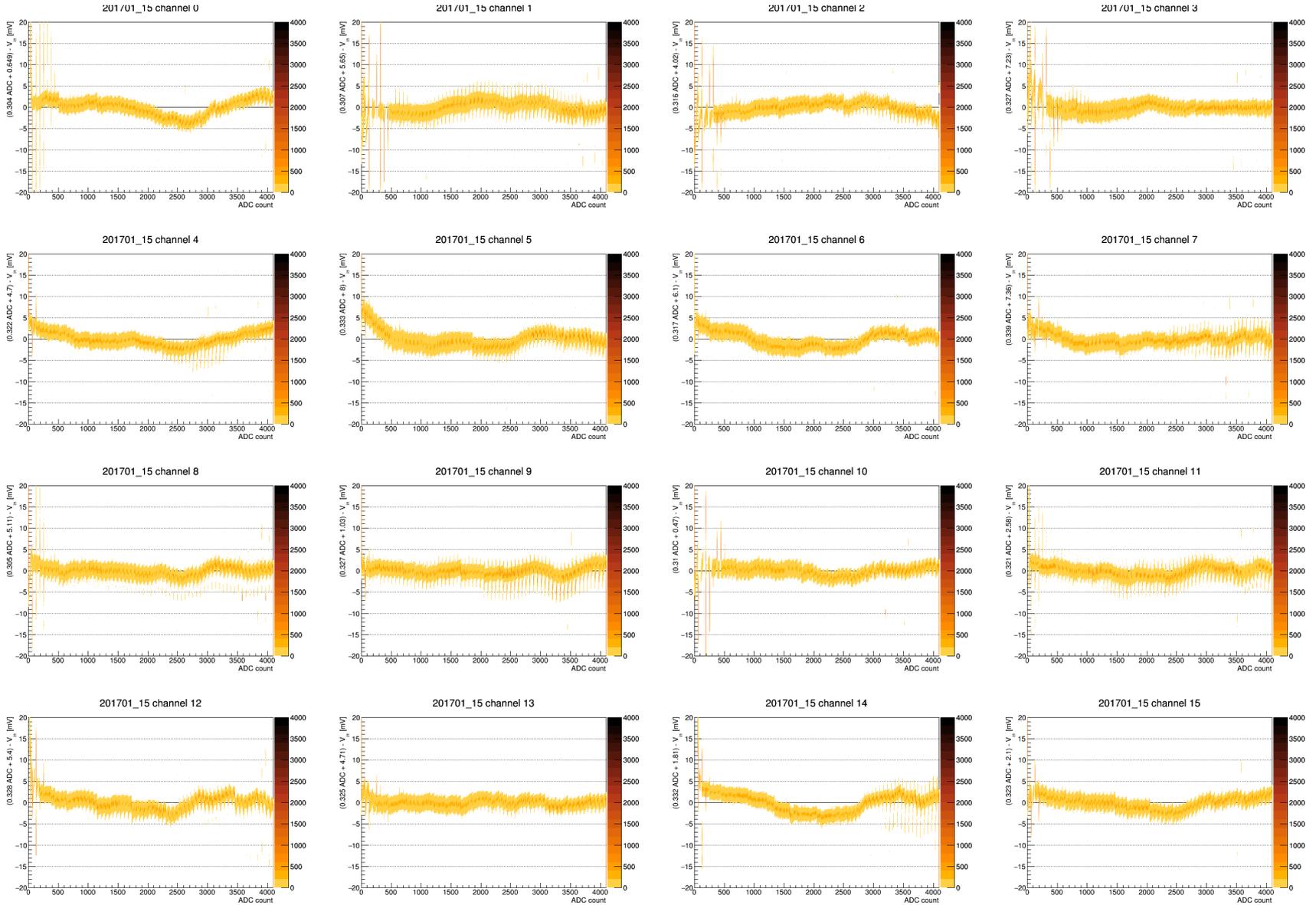
ADC 10



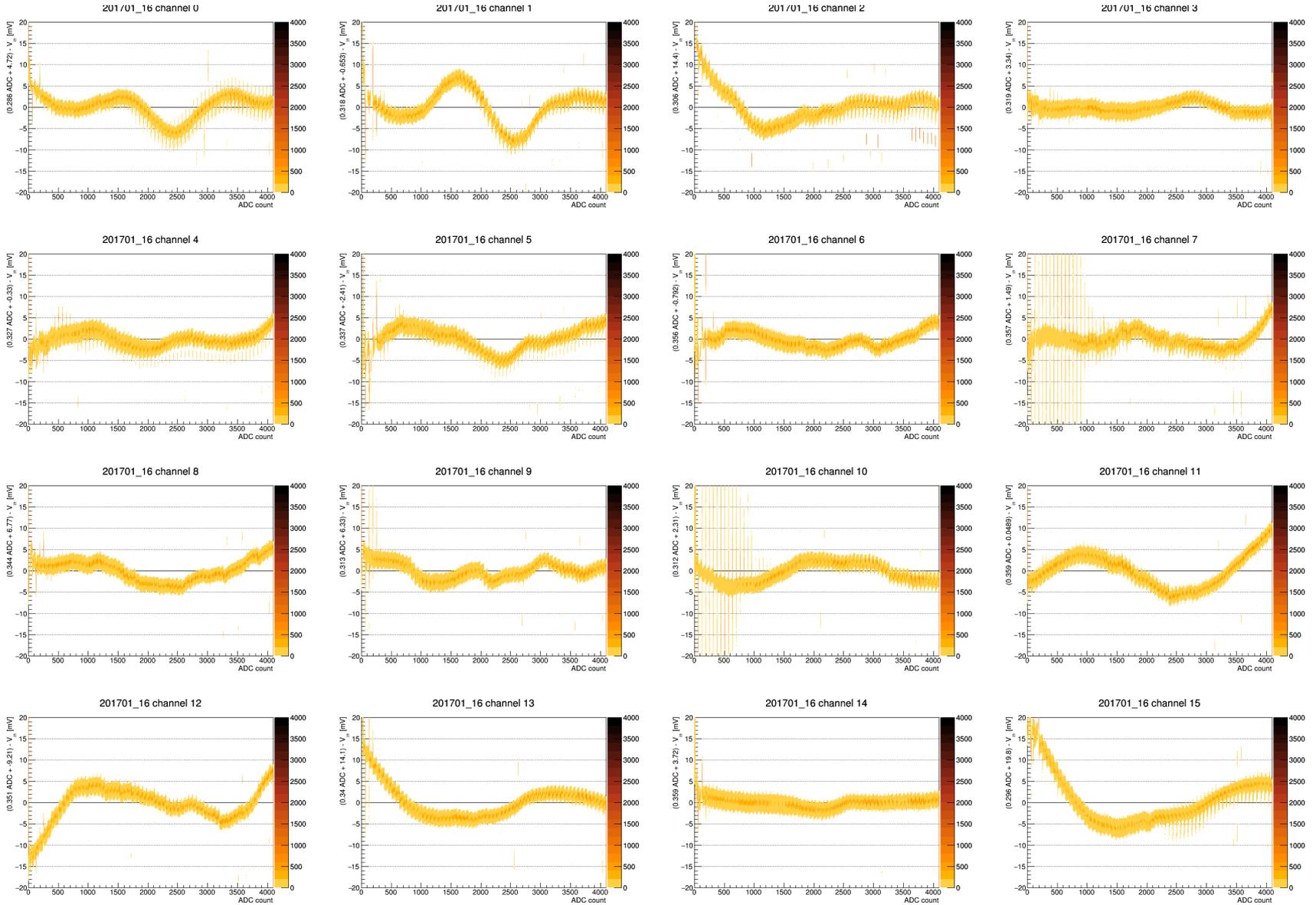
ADC 14



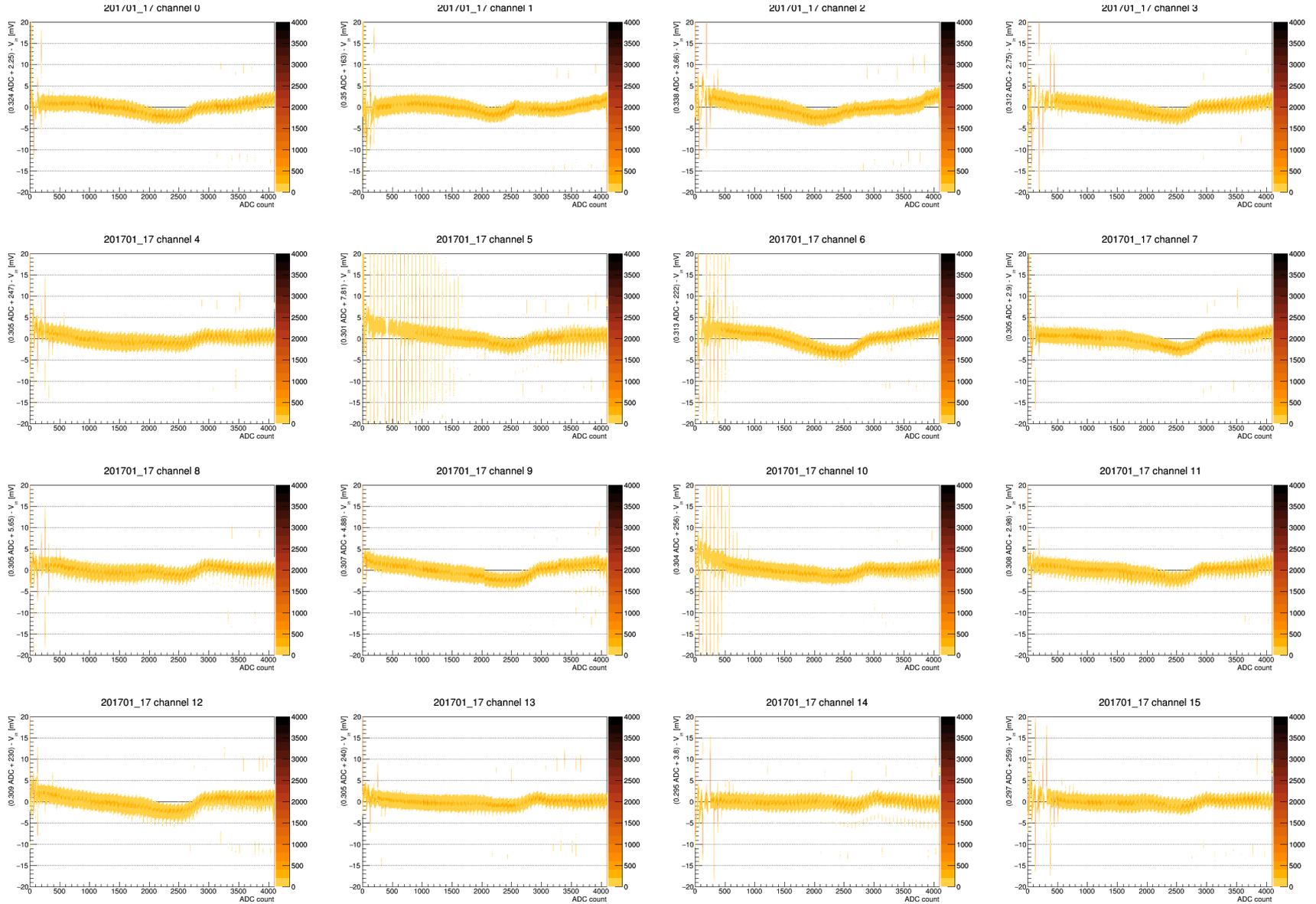
ADC 15



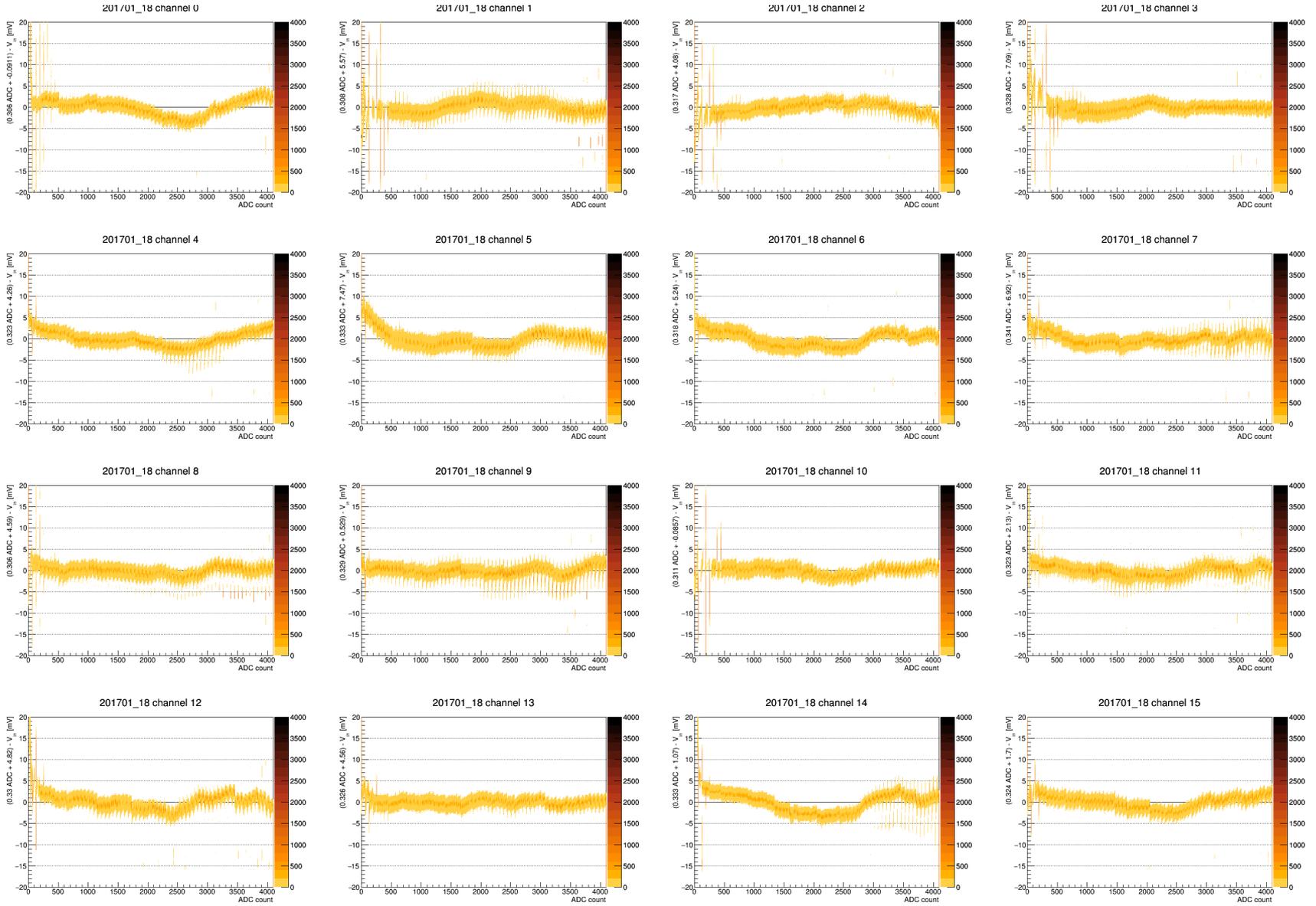
ADC 16



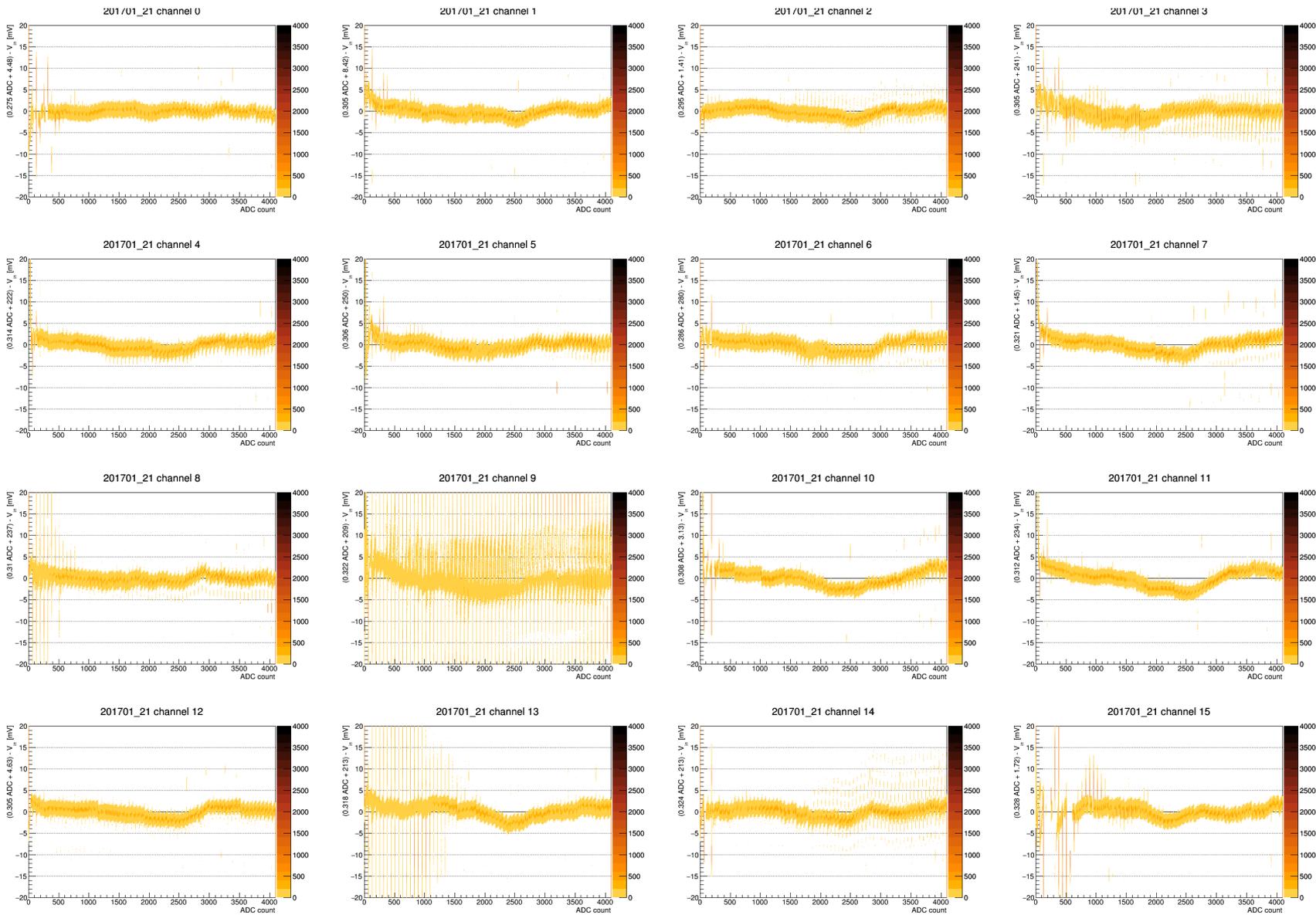
ADC 17



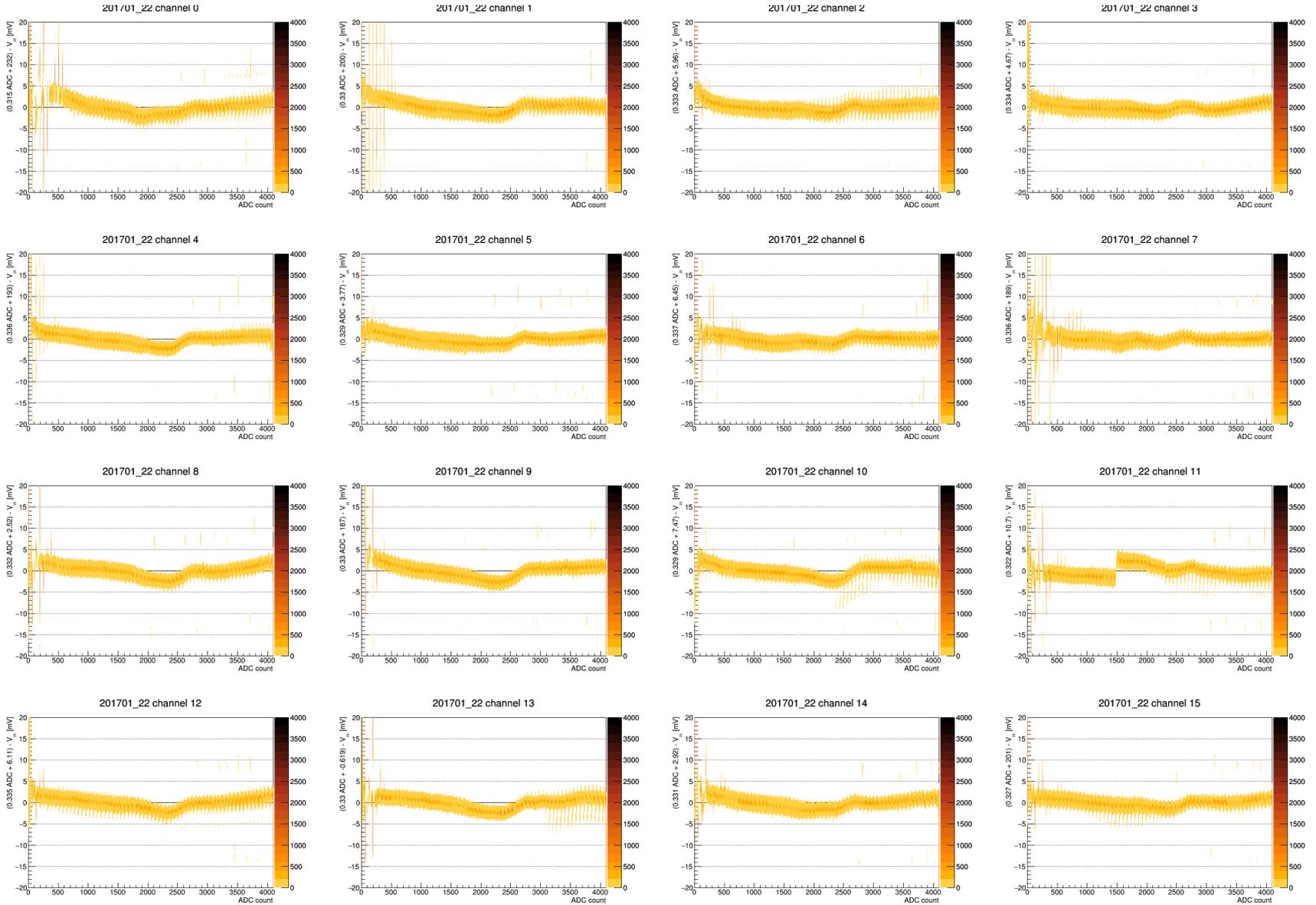
ADC 18



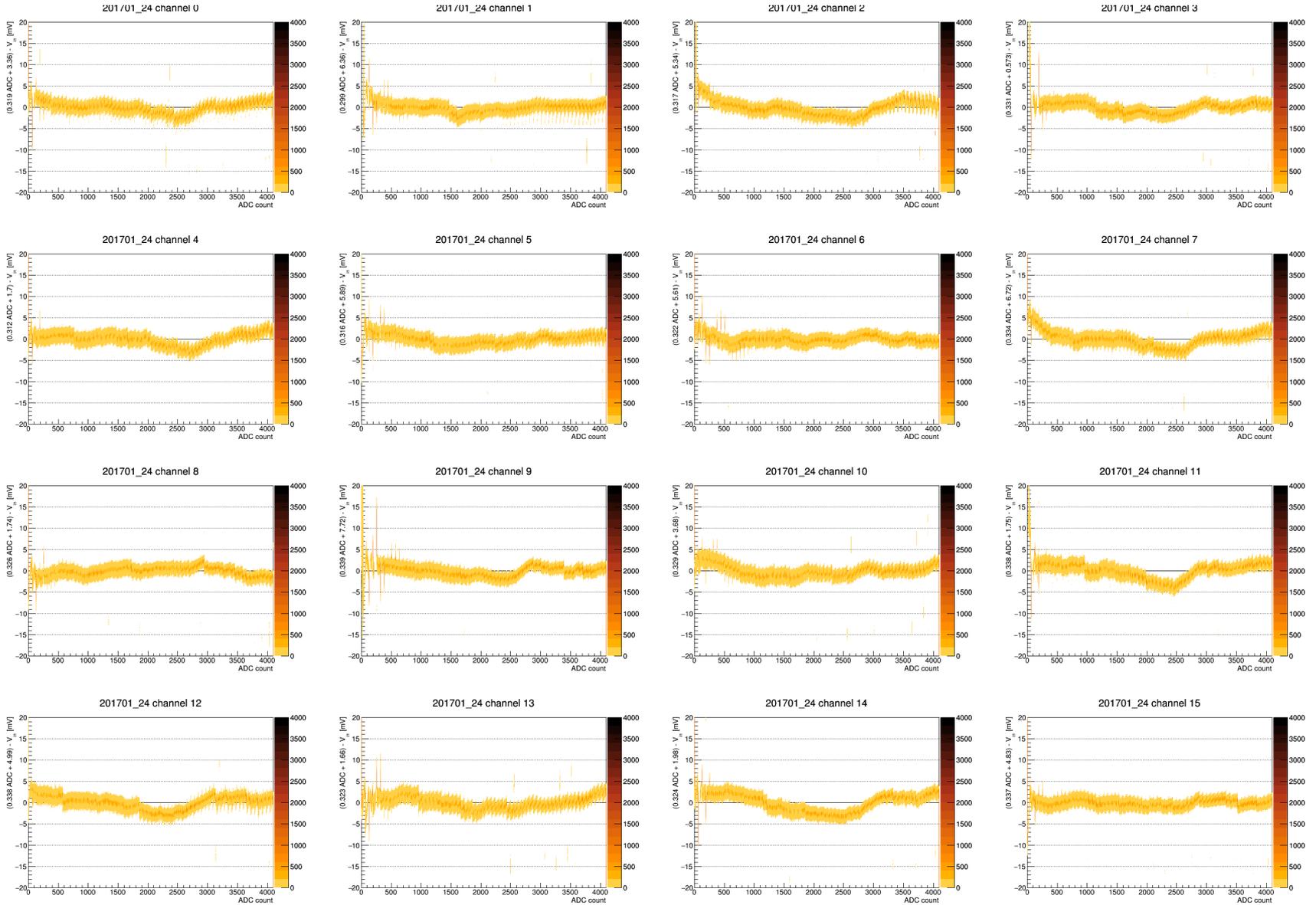
ADC 21



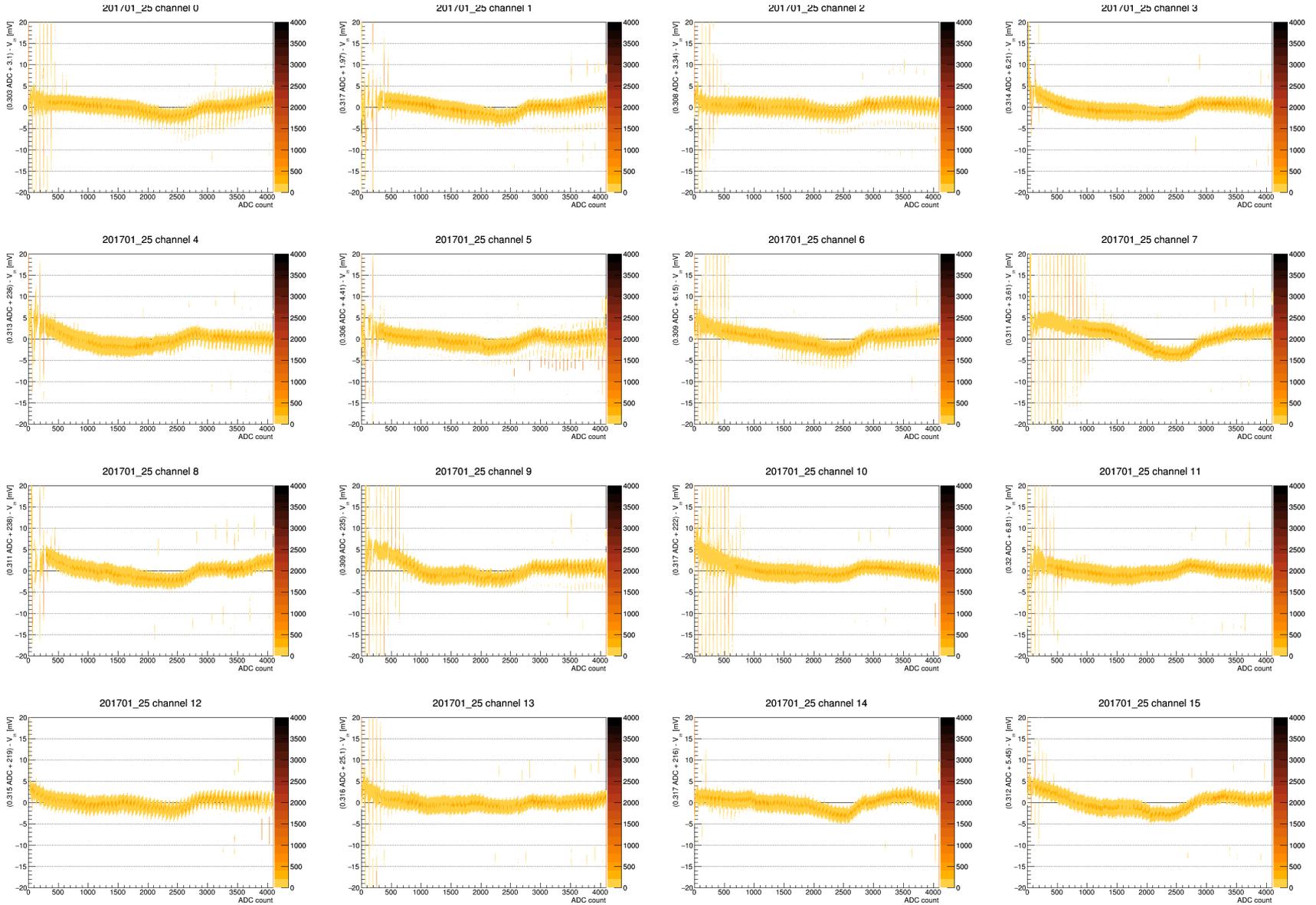
ADC 22



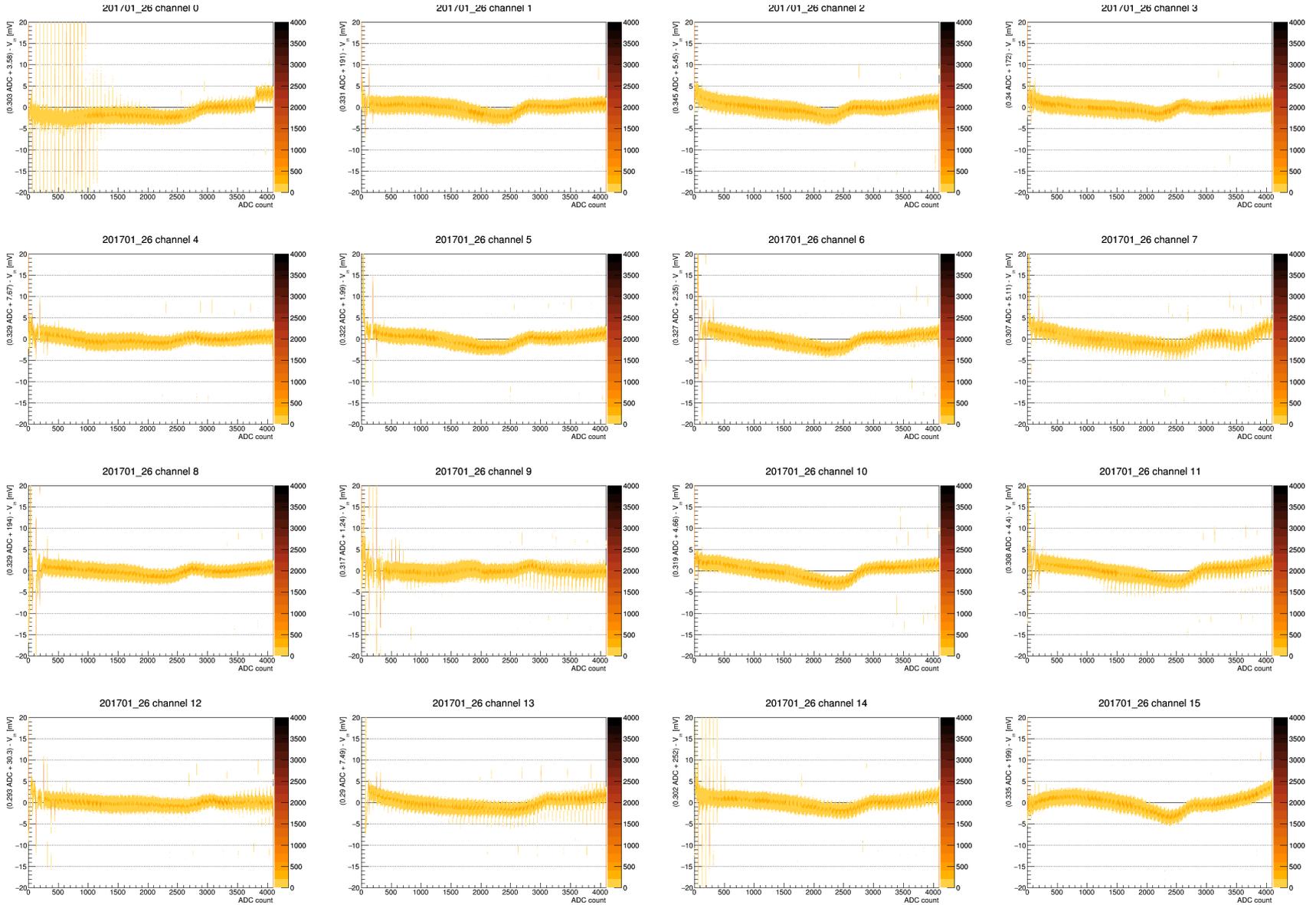
ADC 24



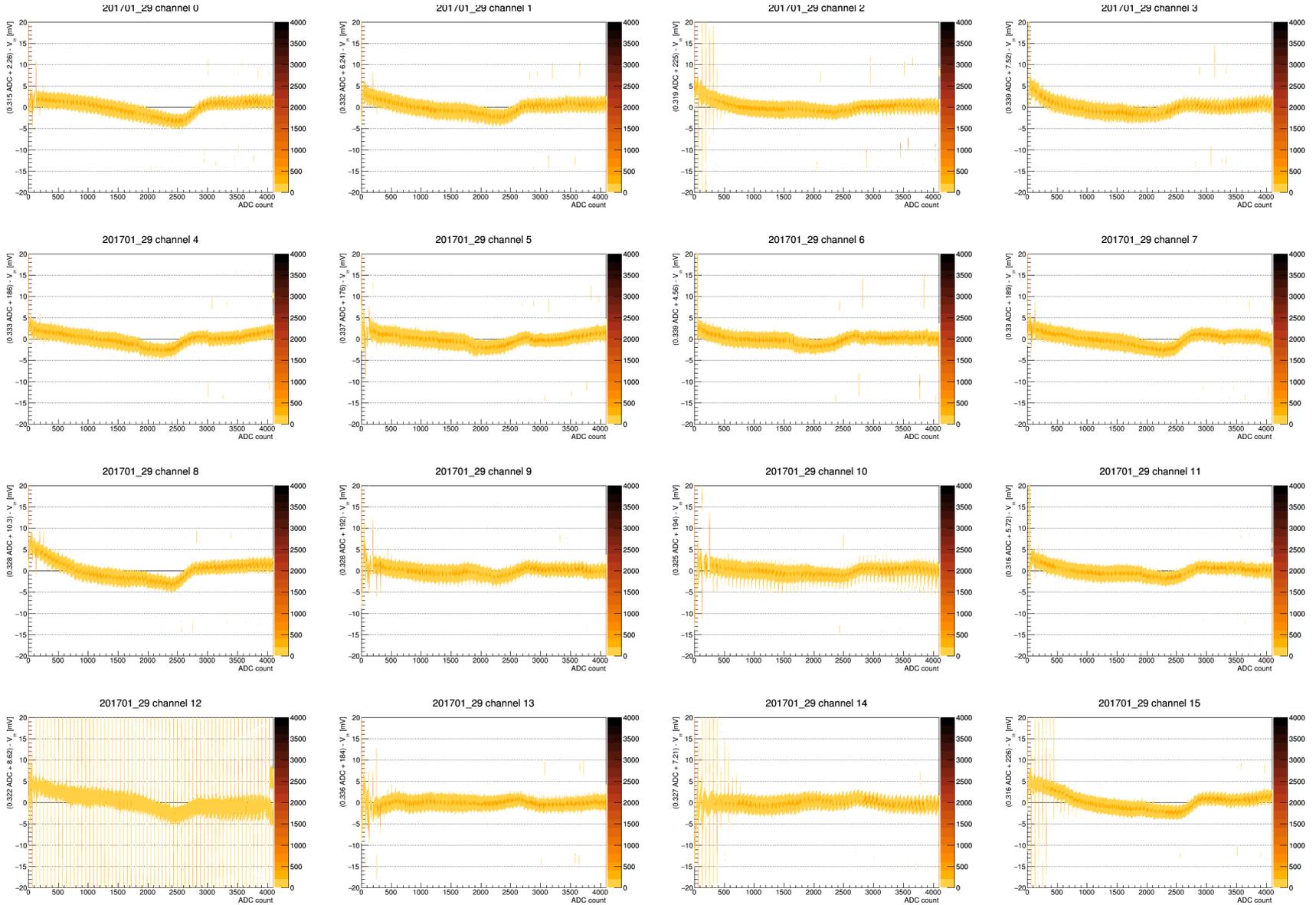
ADC 25



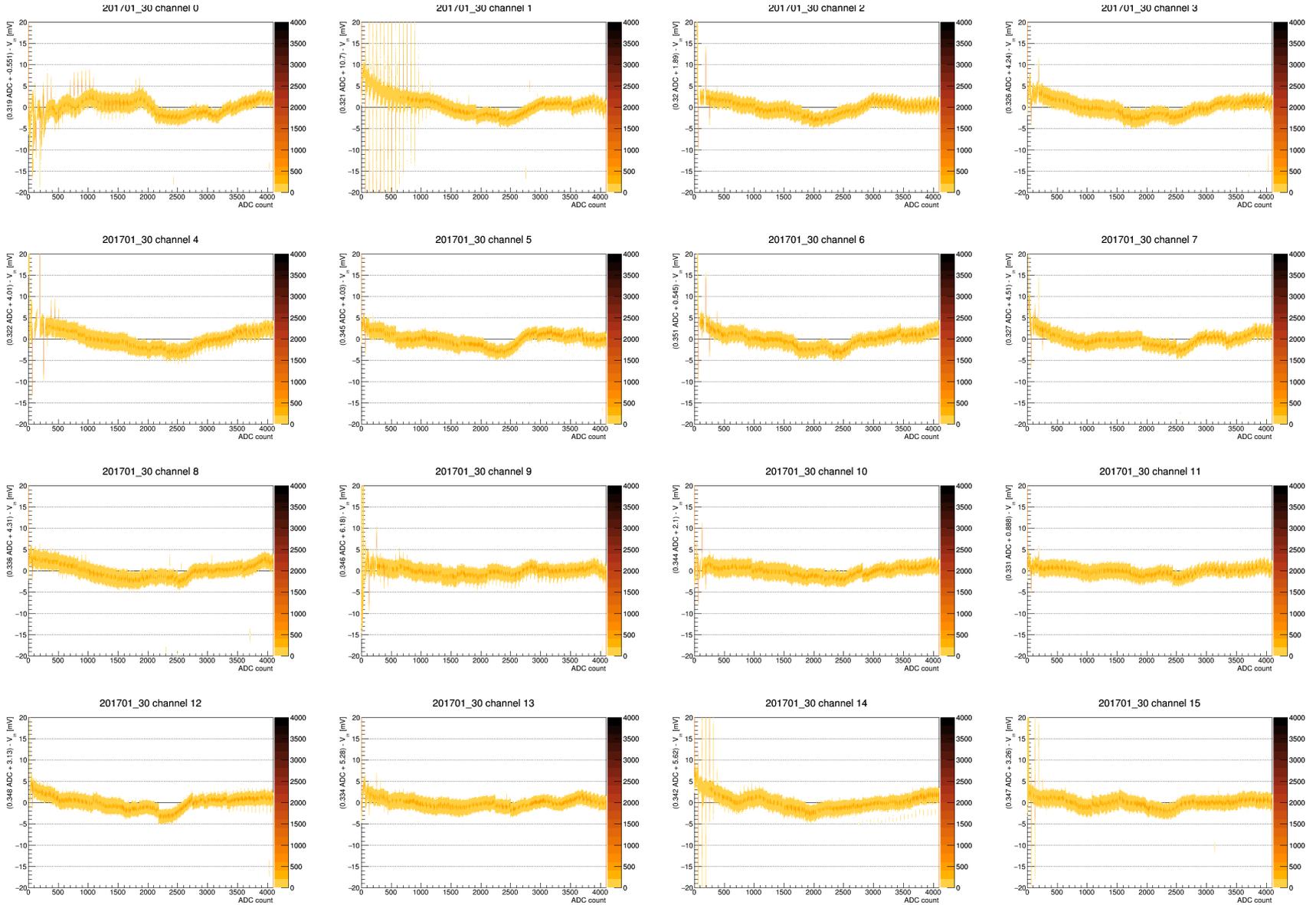
ADC 26



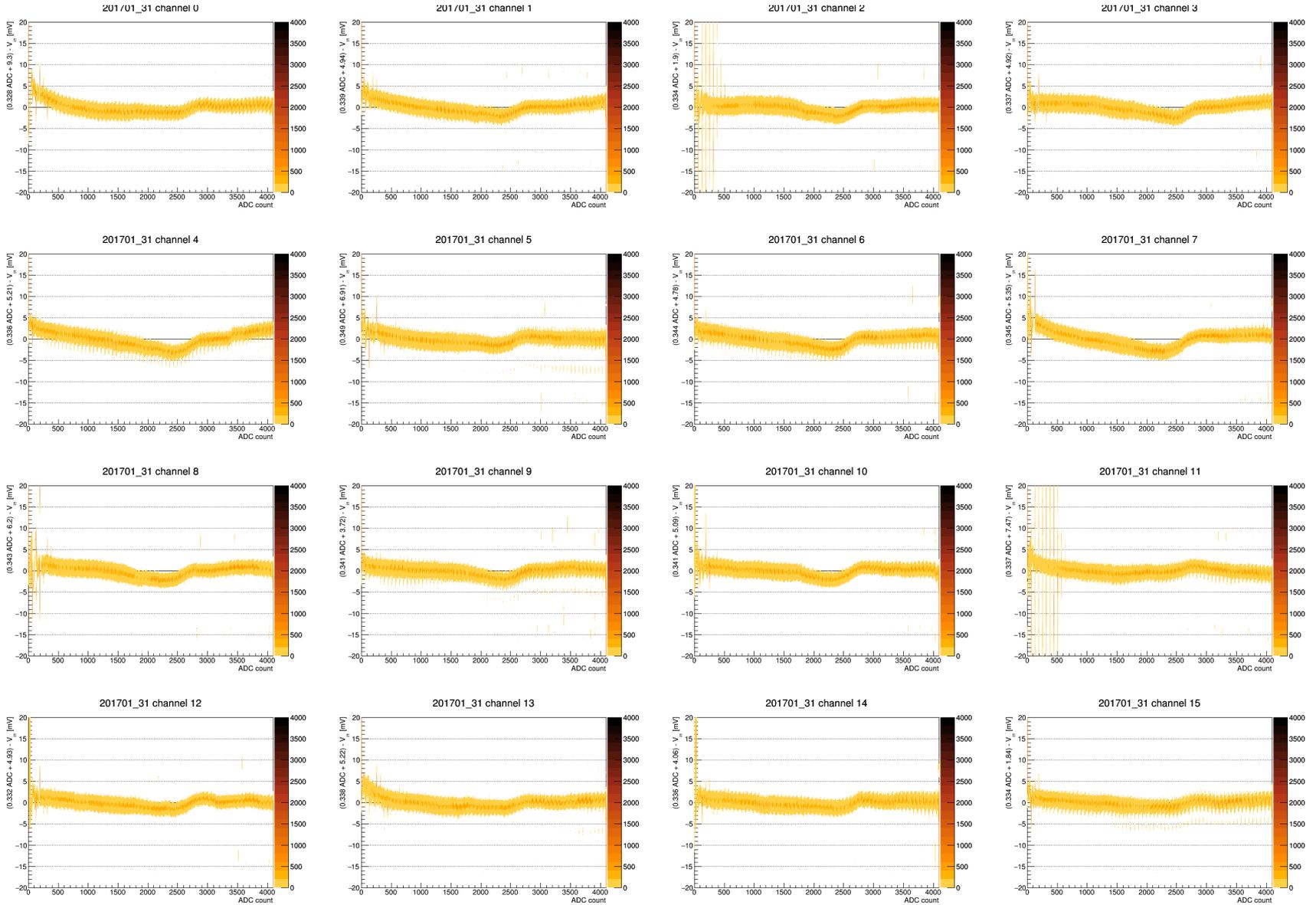
ADC 29



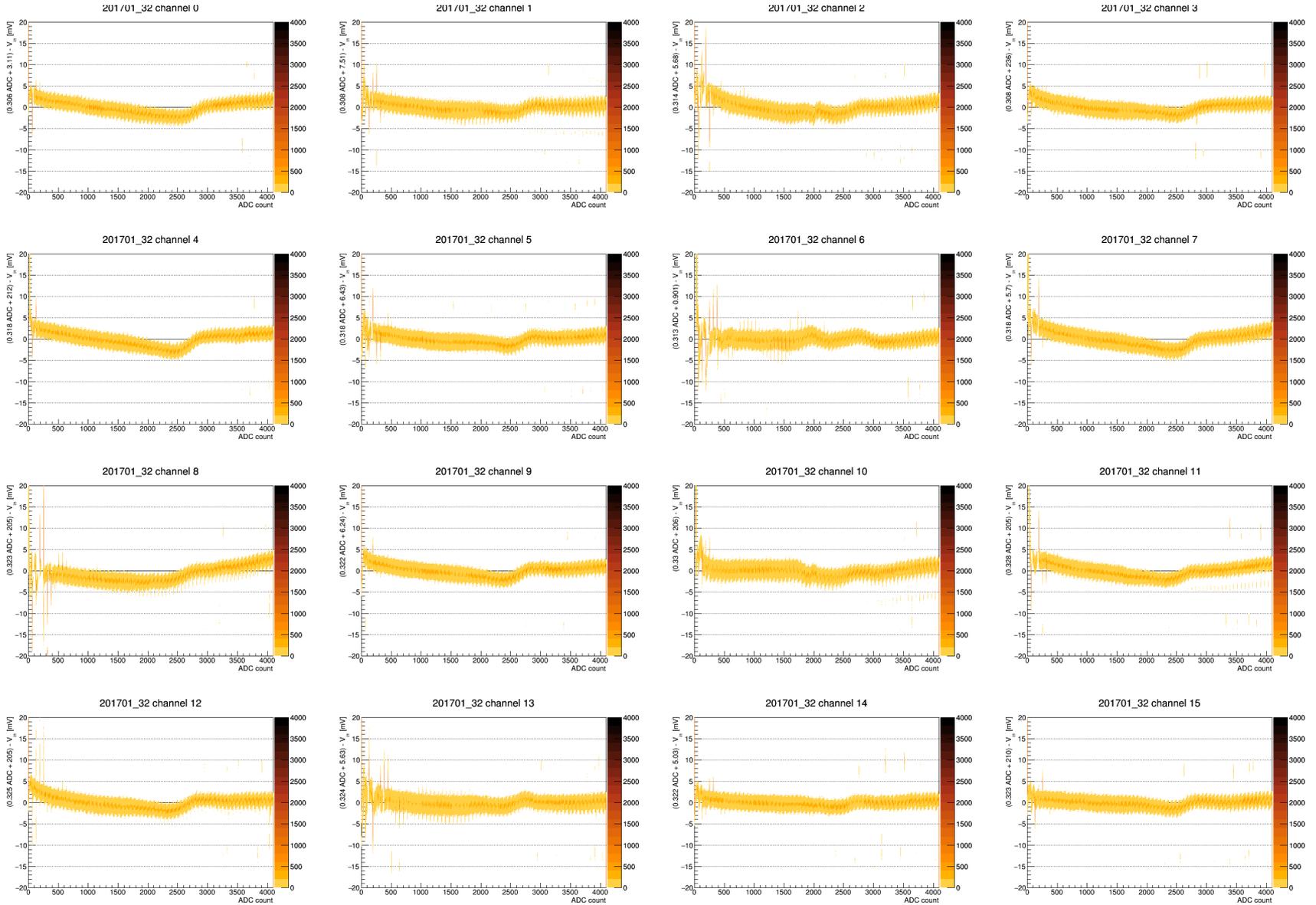
ADC 30



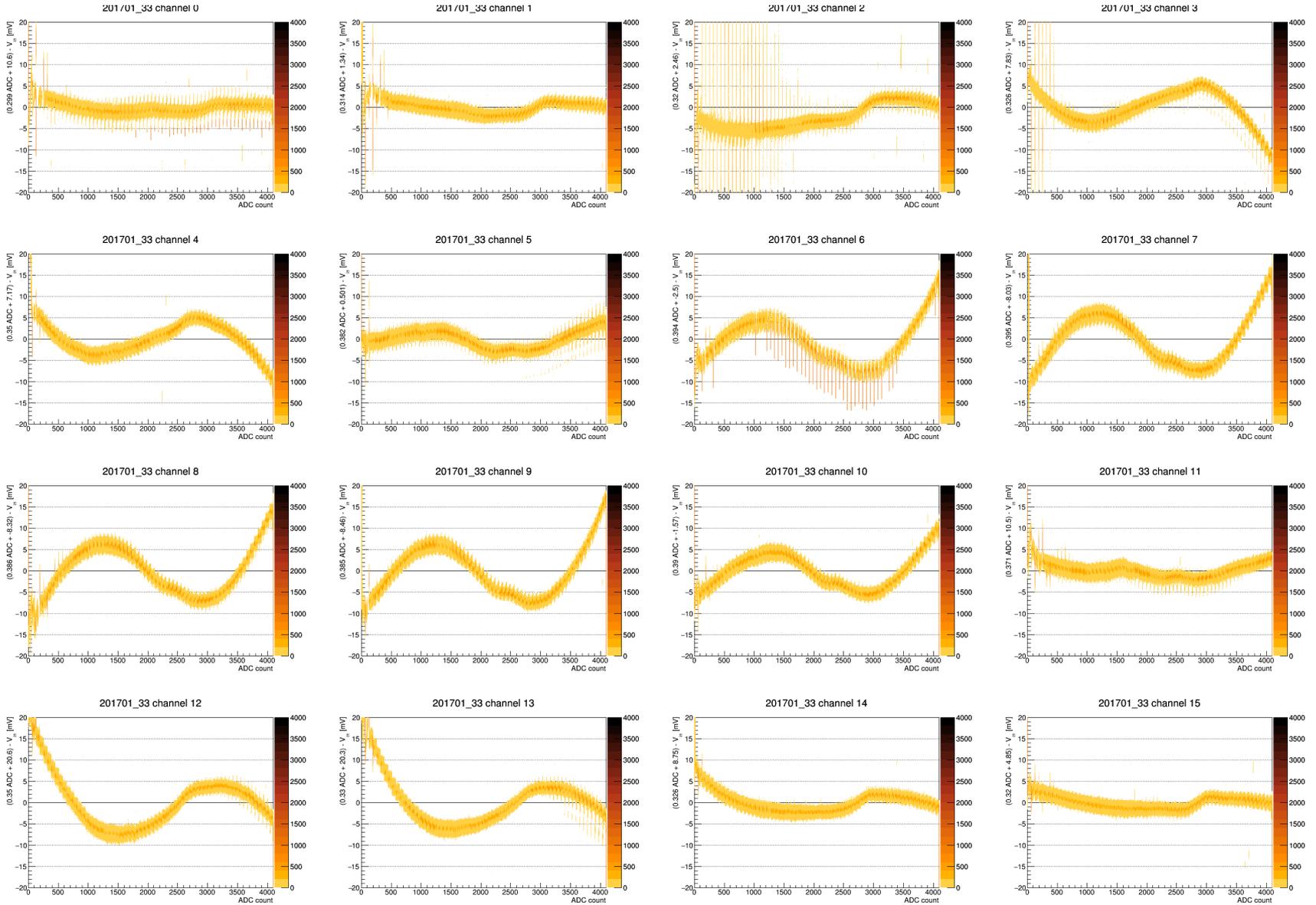
ADC 31



ADC 32



ADC 33



ADC 35

